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MEMRISTOR EFFECT IN HETEROSTRUCTURES BASED ON GALLIUM NITRIDE NANOWIRES ON SILICON

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Abstract. In this work, experimental and theoretical studies of diode heterostructures based on GaN nanowires synthesized on silicon have been carried out. Current-voltage measurements showed the typical backward diode behavior in the range from −3 to +3 V and the appearance of a hysteresis loop at greater biases. It was shown for the first time that the effect of bipolar resistive switching could be observed in such structures. The ability of the corresponding memristor cells to remain their state for a long time (not less than 65 hrs) under normal conditions, as well as to bear long read cycles without loss of information were demonstrated.

Keywords: memristor effect, resistive switching, gallium nitride, nanowires, silicon

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МЕМРИСТОРНЫЙ ЭФФЕКТ В ГЕТЕРОСТРУКТУРАХ НА ОСНОВЕ НИТЕВИДНЫХ НАНОКРИСТАЛЛОВ НИТРИДА ГАЛЛИЯ НА КРЕМНИИ

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Аннотация. Проведены экспериментальные и теоретические исследования диодных гетероструктур на основе нитевидных нанокристаллов GaN, синтезированных на кремнии. Измерения вольтамперных характеристик показали закономерность их

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поведения, характерную для обращенных диодов, в диапазоне от −3 до +3 В, и появление петли гистерезиса при бульших смещениях. Впервые было показано, что в таких структурах может наблюдаться эффект резистивного переключения биполярного типа. Продемонстрирована способность соответствующих мемристорных ячеек сохранять свое состояние в течение не менее 65 ч при нормальных условиях, а также выдерживать продолжительные циклы считывания без потери информации.

Ключевые слова: мемристорный эффект, резистивное переключение, нитрид галлия, нитевидные нанокристаллы, кремний

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Introduction

Advances in information technology, especially artificial intelligence, demand higher performance from computing systems, which inevitably leads to increased power consumption. The scientific community is actively exploring ways to address the challenges associated with transistor density in integrated circuits and reducing their power consumption. It is well known that the physical limit of integration is expected to be reached in the coming years [1]; further progress will require either optimizing the existing architecture or introducing new architectures and methods.

One of the approaches to overcoming these obstacles is to perform computations entirely within the system's memory. This approach is called In-Memory-Computing (IMC) and offers several advantages by minimizing both the time and energy costs of communication between the processor and the memory. A promising implementation of this idea is resistive random-access memory (RRAM), which is based on a passive circuit element called a memristor (a portmanteau of memory and resistor) [2]. The key feature of memristors is their ability to change and 'remember' their resistance depending on the history of applied voltage. The memristor effect was reported in various material systems, for example, metal oxides (including multilayer structures) [3, 4], perovskites [5], two-dimensional materials [6], organic compounds [7], and semiconductor heterostructures [8].

Among semiconductor materials, gallium nitride (GaN) deserves special attention, as it is used to develop and manufacture modern components for power electronics, optoelectronics, and microwave electronics. GaN has also been the subject of intensive research in the context of memristive devices [9–11]. Furthermore, fabricating GaN as nanowires (NWs) rather than planar layers ensures high crystalline quality of the nanostructures on the one hand, and facilitates the creation of nanoscale semiconductor devices on the other hand. Moreover, GaN NWs with high crystalline quality can be grown directly on silicon without buffer layers [12–15], which is important for integration with the accessible and well-established silicon technology.

This work presents results demonstrating for the first time the memristor effect in a GaN NWs/Si tunnel heterostructure.

Synthesis and preparation of structures

Gallium nitride NWs were grown on *p*-type silicon substrates by molecular beam epitaxy (MBE) using an inductively coupled plasma nitrogen source and a gallium effusion cell installed in a Veeco GEN III system. Silicon wafers were prepared and a protective oxide layer was formed by a modified Shiraki method [16]. Next, the oxide was removed in the growth chamber by

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thermal annealing to a temperature of 800–850 °C for half an hour under ultrahigh vacuum, with the formation of a reconstructed Si(111) 7 × 7 surface, confirming its high purity. After that, the silicon surface was nitrided at 550 °C in an activated nitrogen plasma flux (at a rate of 10 ml/min) with the set power of 500 W. Then, the surface of the wafer was covered with a monatomic layer of aluminum, turning into an aluminum nitride (AlN) upon subsequent exposure to nitrogen and forming a selective mask for synthesizing GaN NWs. A Ga-polar GaN layer forms on the AlN surface, which then turns into a coalescing island layer, while NW synthesis occurs at the grain boundaries between individual domains of the AlN layer [17].

Further growth of GaN NWs was carried out at a temperature of 850 °C. Importantly, the AlN mask was chosen with a specific purpose. As the aluminum layer is deposited onto the epitaxial wafer, it partially diffuses into the silicon, forming a highly doped *p*-type region near the surface. In turn, to ensure *n*-type conductivity of the NWs, they were additionally doped with silicon during the growth process. Together, this allows to reduce the thickness of the space charge region at the GaN/Si interface and enhance the influence of tunneling processes on current flow in this structure.

The morphology of the as-grown structures was studied using a Zeiss Supra 25 scanning electron microscope (SEM) (Fig. 1, *a*, *b*). The NWs have a conical shape typical for these growth conditions, which widens with distance away from the wafer. In addition to the NW array, the SEM images show the presence of a parasitic network layer of Ga-polar GaN located between individual NWs, which is typical for synthesis with an AlN mask. The height of the NWs was up to 700 nm with the average diameter varying from 50 to 150 nm. The estimated NW surface density was about 10 μm^{-2}.

The next stage of the work consisted of the production of experimental samples based on the epitaxial structures grown. After a thin aluminum film was deposited on the back side of the Si substrate to form a bottom contact, the sample was processed in a Jipelec JetFirst 100 rapid

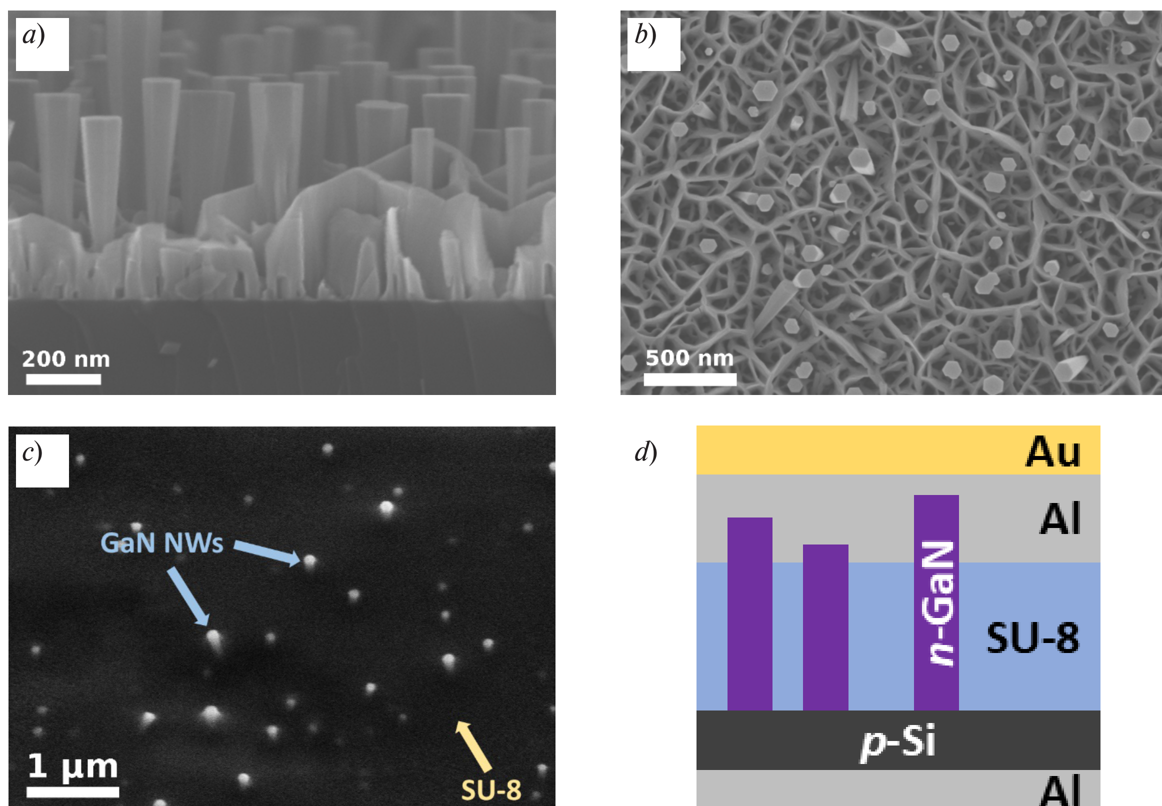

Fig. 1. SEM images of as-grown *n*-GaN NWs/*p*-Si structure (*a*–*c*) and schematic diagram of this structure after full post-growth processing cycle (*d*); cross-sectional cleave (*a*), top view (*b*), 45° view after SU-8 etching in oxygen plasma (*c*)

thermal annealing system at 300 °C for 10 minutes in a nitrogen atmosphere. A dispensing pipette was then used to fill the space between the NWs with a photocurable epoxy resin (SU-8), followed by spin coating, UV exposure, and a final hard bake at 250 °C. To remove SU-8 from the NW tips (to subsequently form ohmic contacts), the structure was partially etched in oxygen plasma using PiNK Plasma system V15-G (400 W, 60 sccm, 15 min). The top contact was prepared as an array of round Al/Au mesas with a diameter of 100 μm, obtained using laser lithography and vacuum deposition. The total contact thickness was 250 nm. Metallization was carried out in the BOC Edwards Auto 500 thermal resistance evaporator for both contacts. Directly before loading into the chamber, the corresponding surfaces were treated in each case with solutions of hydrofluoric acid and hydrochloric acid (for Si and GaN, respectively) to remove the surface oxide. The results of the post-growth process are shown in Fig. 1, *c*, *d*.

Results and discussion

The first stage in the characterization of the prepared mesa samples was the measurement of current–voltage characteristics, carried out at room temperature with a specialized probe station. The positive pole of the Keithley 2401 precision source measure unit was applied to the bottom contact (*p*-Si), and the negative pole was applied to the top contact (*n*-GaN). At first, relatively small voltages were applied to the structure with a gradual expansion of the range (Fig. 2), while measurements were carried out in cyclic mode with the following sweep sequence:

$$-U \rightarrow 0 \rightarrow +U \rightarrow 0 \rightarrow -U. \tag{1}$$

As seen from the graphs in Fig. 2,*a*, the *I*–*V* curve in the range from -3 to +3 V corresponds to the behavior of the backward diode when the reverse branch opens before the forward one. This indicates that the doping degrees of the layers forming the *p*–*n* junction are selected so that the bottom of the GaN conduction band in the equilibrium state is approximately at the same energy level as the top of the Si valence band [18].

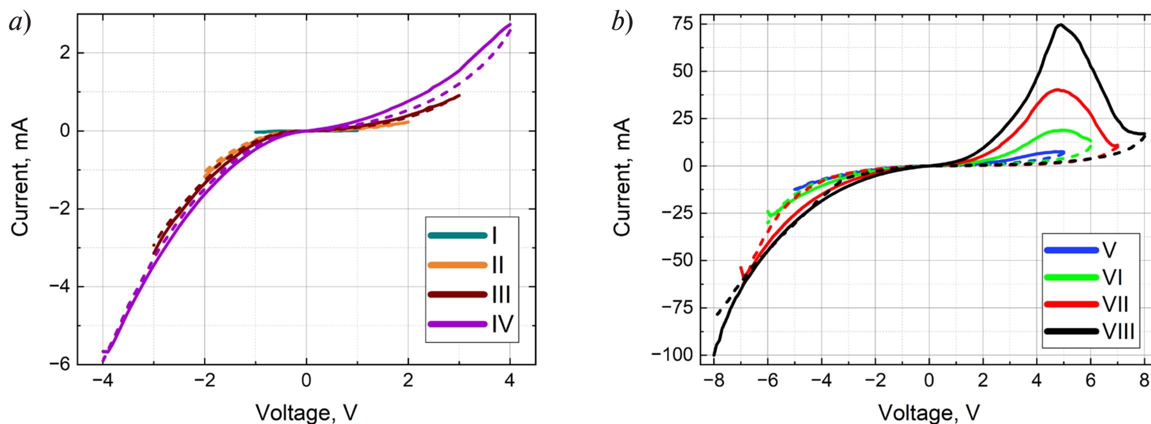

Fig. 2. Sixteen *I*–*V* characteristics measured in mode (1) (solid lines) and in the opposite direction ($+U \rightarrow -U$) (dashed lines) for one mesa of the prepared structure
The colored curves correspond to measurements I–IV (*a*) and V–VIII (*b*)

With a further increase in the applied voltage (above 5 V), a section of negative differential resistance appears, as well as hysteresis in both the forward ($-U \rightarrow +U$) and reverse ($+U \rightarrow -U$) sweep directions (Fig. 2,*b*).

For a more complete picture, a similar experiment was conducted for five other mesas (numbered C2R5–C2R9). In this case (Fig. 3), the measuring cycle with start and end at zero voltage consisted of four consecutive sections, collectively covering the range from -8 to +8 V. As follows from Fig. 3, all mesas exhibit hysteresis, while the *I*–*V* curves coincide well over the entire range under consideration. Hysteresis in the positive voltage region was observed only after preliminary reverse biasing of the structures (steps 1 and 2), which is consistent with the *I*–*V* curves in mode (1) (solid lines in Fig. 2,*b*). It can be concluded from these results as well as from similar

current–voltage characteristics of other mesas (not shown in the figure) that applying a reverse-bias voltage to the structure for about 10 s (the time required to measure the I–V curve in the range from 0 to −8 V) subsequently leads to a significant increase in the forward current compared to the initial state of the same structure. This behavior is equivalent to a write operation in a memory cell. In turn, applying a forward bias equivalent to step 4 eliminates this effect, restoring the structure to its initial state with lower conductivity (see Figs. 2,*b* and 3). This behavior is reversible, and the structure can be repeatedly switched between two stable states by applying a voltage of the appropriate polarity (forward bias for erasing, reverse bias for writing).

We believe that the physical mechanisms behind this behavior of the given structures are closely related to the specifics of NW synthesis. Aluminum, gallium, nitrogen, and silicon are representatives of different groups of the periodic table and can form a large number of different compounds, including wide-bandgap semiconductors. Thus, thin layers of silicon nitride, silicides, and other compounds can form between the substrate and the GaN NWs during synthesis of the structure; the presence of these layers may affect charge carrier transport between GaN and Si. An important characteristic of wide-bandgap layers is the possible presence of charge centers whose energy levels are located deep in the bandgap of the material and are described by a highly localized wave function (the electron orbital has a small radius). The levels for which the wave function is largely localized within the layer form traps for charge carriers with long lifetimes. Such levels do not participate in transport of charge carriers, but may indirectly affect the charge transfer initiated by Coulomb forces. These states are likely responsible for the observed behavior of the current–voltage curves in the given structure.

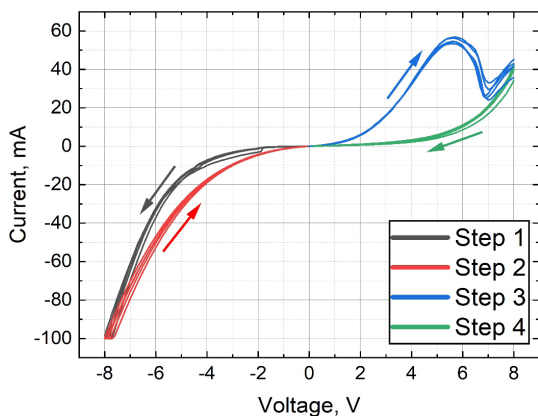

Fig. 3. Superposition of cyclic I–V curves obtained in 0 V → -8 V → 0 V → +8 V → 0 V sweep for five different mesas (C2R5–C2R9)

Fig. 4 shows the band diagrams of the structures corresponding to different steps of measuring the I–V curves marked in Fig. 3. Initially, the band structure of the system considered (see Fig. 4,*a*) corresponds to a certain distribution of charge carriers on isolated centers of the wide-bandgap interface layer (not shown in Fig. 4), determined by epitaxial synthesis and presumably close to equilibrium due to the high growth temperature. The band structure of the system then corresponds to that of the GaN/Si interface, taking into account static corrections caused by local mechanical strains due to the lattice mismatch between GaN and Si, as well as the charge in gallium nitride induced by the piezoelectric effect. When a negative voltage is applied to the semiconductor structure as seen in Fig. 4,*b* (step I in Fig. 3), a possible scenario is that continuum states (allowed bands of gallium nitride and silicon) are located in close proximity on both sides of the isolated centers. The configuration allows charge carriers to tunnel through these centers via the Poole–Frenkel mechanism [19]. This process reduces the lifetime of the states and causes them to recharge until local equilibrium corresponding to the given bias level is reached, which constitutes the write operation. When the applied voltage is switched off (step II in Fig. 3), the carriers again become trapped at deep centers. However, the altered charge distribution at these centers now modifies the Coulomb field, which consequently distorts the band structure of the entire heterointerface (see Fig. 4,*c*). This affects the equilibrium concentration of free charge carriers in GaN and Si near the interface and changes the conditions for their tunneling and recombination. The change in the charge at the isolated centers in the given semiconductor structure corresponds to an increase in current under forward bias (step 3 in Fig. 3). Given the expected doping levels in GaN (on the order of 10^{19} cm^{-3}) and Si (on the order of 10^{20} cm^{-3}), we can conclude that the energy levels of the localized centers lie below the Fermi level in the bandgap. The write operation under negative bias leads to an increase in the positive charge and brings the potential barrier heights at the interface closer together for electrons in GaN and holes in Si, or, in other words, the product of their equilibrium concentrations increases. A further increase in forward bias allows for the diode structure to open (Fig. 4,*d*), leading to a significant rise in the

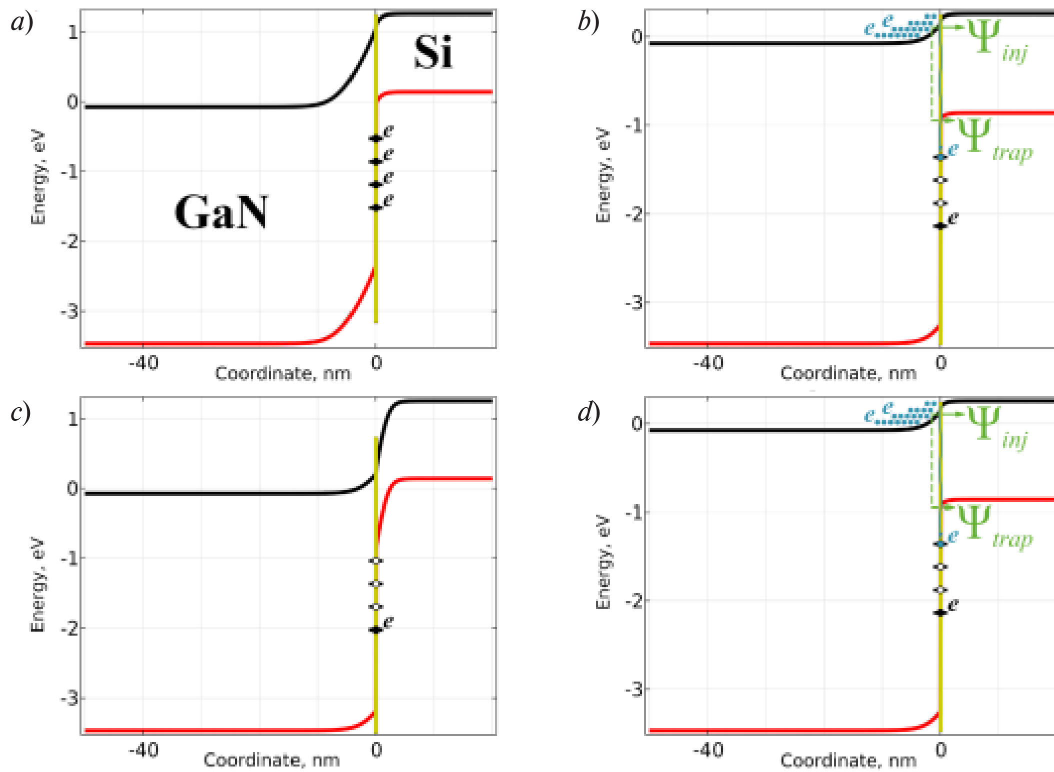

Fig. 4. Band diagrams illustrating the write-erase cycle in the GaN/Si heterostructure: initial state $U = 0$ (*a*), write $0 \to -U$ (*b*), write $-U \to 0$ (*c*), erase $0 \to +U$ (*d*); Ψ_{tun}, Ψ_{inj}, Ψ_{trap} are the wave functions of tunneling, system states after injection and trapping of electrons (*e*), respectively

concentration of free charge carriers near the interface. Accordingly, recharging of isolated centers occurs, either through the Shockley–Read–Hall recombination involving free carriers injected into the allowed band of the wide-bandgap interface layer between GaN and Si, or through carrier trapping at other energy levels within the bandgap of this layer, followed by recombination with carriers located at the isolated centers. This completes the erase operation. Importantly, applying voltages below certain thresholds (either the threshold for carrier tunneling via the Poole–Frenkel mechanism or the threshold for activating the Shockley–Read–Hall recombination mechanism) does not alter the charge distribution at the isolated centers, therefore leaving the system state unchanged. In our case, this situation is observed experimentally: the I–V curves in Fig. 2,*a* show no hysteresis in the range from –3 to +3 V.

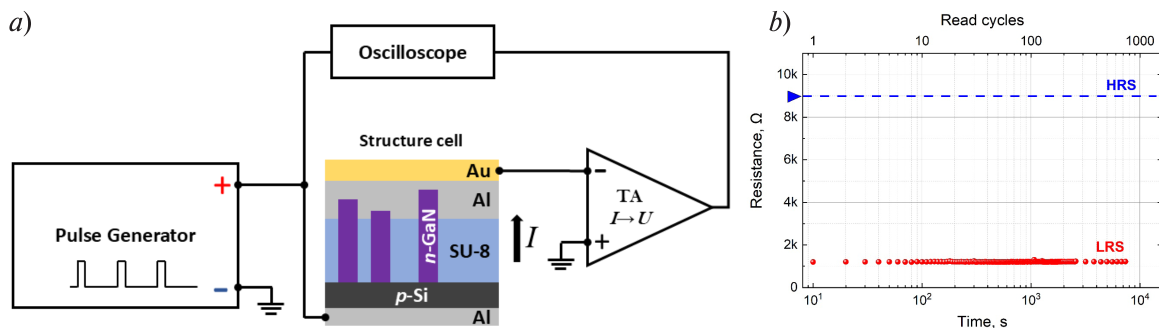

Fig. 5. Memristive properties of cell C2R4 65 hours after writing a logic 1: schematic diagram of measurement circuit (*a*), time sweep of sequential resistance read pulses with $V_{read} = 0.5$ V at a frequency of 0.1 Hz (*b*); HRS, LRS are the high and low resistive states, corresponding to logic 0 and 1 levels, respectively

Let us compare the results obtained with the data available in the literature. For example, interface-type switching in memristors is mentioned in [20]. Resistive switching in metal/perovskite structures depending on the polarity of the applied voltage was observed in [21, 22]. The authors interpret this effect within the framework of a model with trap states at the interface. Memristor structures based on charge traps are considered in [23, 24]. Theoretical studies were also carried out on resistive switching in memristors based on the interface trap model [25]. Thus, we suppose that bipolar resistive switching can occur in the given samples (switching of states is achieved by applying voltages of opposite polarities). To the best of our knowledge, this effect has been established for the first time for GaN NWs/Si heterostructures.

The memristor properties of the heterostructures were analyzed at the next stage. Since writing a logic 1 (or the low resistive state, LRS) is performed by applying a reverse bias voltage, we applied a −8 V bias for 10 s to one of the mesas previously unused in the measurements (C2R4). Next, the structure was disconnected from the external circuit and left undisturbed for 65 hours. After this time, the measurement probes were reconnected, and a series of 738 read cycles was performed using the standard measurement setup (Fig. 5,*a*). Reading was performed using +0.5 V rectangular voltage pulses with a frequency of 0.1 Hz (pulse duration was 1 ms). The current passing through the structure was converted into voltage by a transimpedance amplifier (TA in Fig. 5) and recorded by an oscilloscope. For the first 198 cycles, the voltage readings at the TA output were recorded every 10 s; for the next 60 cycles, every minute; and for the last 480 cycles, every 10 min. The measurement results are shown in Fig. 5,*b*.

Since the cells are initially in HRS, corresponding to a logic 0, the forward branch of the $I-V$ curve was measured up to 5 V before writing a logic 1. According to this dependence, the resistance value of 9 kOhm, corresponding to HRS was found for the read voltage (marked with the blue line in Fig. 5,*b*).

As can be seen, the resistance value of the cell practically does not change throughout the entire reading time, remaining at the level of 1.2 kOhm, which is more than 7 times lower relative to HRS. A continuous forward bias of +8 V was applied to the cell after this experiment; the cell consequently returned to its initial high resistive state. To verify the return to the initial state, the $I-V$ curve was measured again and compared with the one obtained before writing a logic 1 into the cell. Thus, it is confirmed that the structures considered can memorize and store logic variables.

Conclusion

We studied heterostructures based on *n*-GaN nanowire arrays grown on *p*-Si by molecular beam epitaxy using an aluminum seed layer to initiate nanowire growth. Ohmic contacts were formed on the vertically aligned NW arrays using post-growth processing methods, patterned into circular mesas with a diameter of 100 μm. Based on current−voltage measurements under cyclic voltage sweeps, we observed, for the first time, a bipolar resistive switching effect in these structures. Furthermore, we demonstrated that these structures can retain a low resistive state for a considerably long time (at least 65 hours) and withstand multiple read cycles (738 cycles) without data loss.

Thus, heterostructures incorporating *n*-GaN nanowires on *p*-Si can exhibit memristive properties, which we attribute to the presence of tunable charge centers near the heterointerface, influencing the conductivity of the system via field effects.

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