Conference paper
UDC 621.315.592
DOI: https://doi.org/10.18721/JPM.171.127

Thermally stable connecting GaAs/AlGaAs tunnel diodes for laser radiation multi-junction photoconverters

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Abstract. A new type of thermally stable GaAs/AlGaAs tunnel diode with an intermediate *i*-layer is proposed as a connecting element between photoactive sub-elements in monolithic multijunction photoconverters. In the temperature range of (25–80) °C, the current-voltage characteristics for two types of n^{++}-GaAs(δSi)/p^{++}-$Al_{0.4}Ga_{0.6}As$(C) and n^{++}-GaAs(δSi)/*i*-GaAs/p^{++}-$Al_{0.4}Ga_{0.6}As$:(C) structures of connecting tunnel diodes were studied. The temperature dependences of the peak tunneling current density – (J_p) and differential resistance – (R_d) were obtained. In the samples of tunnel diodes of the structure with an *i*-layer, an order of magnitude higher J_p values and an order of magnitude lower R_d values were obtained, with higher temperature stability than in the samples of the structure without an *i*-layer. The results obtained are useful in the development and creation of monolithic multijunction photoconverters of high-power laser radiation.

Keywords: tunnel diode, photoactive *p-n* junctions, multijunction laser radiation photoconverters, current-voltage characteristics, peak tunnel current density, differential resistance

Citation: Kalinovskii V.S., Maleev N.A., Vasilyev A.P., Kontrosh E.V., Tolkachev I.A., Prudchenko K.K., Ustinov V.M., Thermally stable connecting GaAs/AlGaAs tunnel diodes for laser radiation multi-junction photoconverters, St. Petersburg State Polytechnical University Journal. Physics and Mathematics. 17 (1.1) (2024) 165–170. DOI: https://doi.org/10.18721/JPM.171.127

Материалы конференции
УДК 621.315.592
DOI: https://doi.org/10.18721/JPM.171.127

Термостабильные соединительные туннельные диоды GaAs/AlGaAs для многопереходных фотопреобразователей лазерного излучения

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Аннотация. Предложен новый тип термостабильного GaAs/AlGaAs туннельного диода с промежуточным *i*-слоем, как соединительный элемент между фотоактивными суб-элементами в монолитных многопереходных фотопреобразователях лазерного излучения. В температурном диапазоне (25–80) °С исследованы вольтамперные характеристики двух типов структур соединительных туннельных диодов: n^{++}-GaAs(δSi)/p^{++}-$Al_{0.4}Ga_{0.6}As$(C) и n^{++}-GaAs(δSi)/*i*-GaAs/p^{++}-$Al_{0.4}Ga_{0.6}As$:(C). Получены температурные зависимости основных параметров ТД: плотности пикового туннельного тока – (J_p) и дифференциального сопротивления – (R_d). В образцах туннельных диодов структуры с *i*-слоем, получены на порядок большие значения J_p и на порядок меньшие значения R_d, с более высокой температурной стабильностью, чем в образцах структуры без *i*-слоя. Полученные результаты полезны при разработке и создании монолитных многопереходных фотопреобразователей мощного лазерного излучения.

Ключевые слова: туннельный диод, фотоактивные *p-n* переходы, многопереходные лазерные фотопреобразователи, вольтамперные характеристики, пиковое значение плотности туннельного тока, дифференциальное сопротивление

Ссылка при цитировании: Калиновский В.С., Малеев Н.А., Васильев А.П., Контрош Е.В., Толкачев И.А., Прудченко К.К., Устинов В.М. Термостабильные соединительные туннельные диоды GaAs/AlGaAs для многопереходных фотопреобразователей лазерного излучения // Научно-технические ведомости СПбГПУ. Физико-математические науки. 2024. Т. 17. № 1.1. С. 165–170. DOI: https://doi.org/10.18721/ JPM.171.127

Introduction

Improving the parameters of monolithic multijunction photoconverters (MJ PCs) of laser radiation [1] is associated with an increase in the number of photoactive sub-elements connected to each other by back-to-back nanosized and optically transparent tunnel diodes (TDs). The process of epitaxial growth of the structure of a monolithic MJ PCs leads to blurring of profiles and mutual compensation, for example, Si and Be dopant atoms in degenerate nanolayers of GaAs/AlGaAs TD, and, as a consequence, to degradation of the current-voltage characteristic of the TD and MJ PCs parameters. A possible solution to eliminate the degradation of the current-voltage characteristic is the use, for example, carbon as an acceptor impurity. Additionally, we proposed the use of an intermediate, undoped *i*-nanolayer of GaAs between the degenerate n^{++} and p^{++} layers [2]. According to previous numerical simulations of n^{++}-GaAs/*i*-GaAs/p^{++}-$Al_xGa_{1-x}As$ ($x \geq 0.2$) TDs, the inclusion of an *i*-nanolayer makes it possible to increase the peak tunneling current density (J_p). Using models of nonlocal band-to-band quantum tunneling and trap assisted tunneling, the nonmonotonic dependence of the tunneling current J_p on the *i*-nanolayer thickness with the presence of a maximum was shown. In addition, the operating temperature of an MJ PCs in the photovoltaic mode when excited by powerful monochromatic radiation can increase up to 80 °C [3, 4], depending on the efficiency of heat removal and the magnitude of the incident optical power. As the operating temperature increases, the connecting TDs in the MJ PCs must provide consistently high J_p values exceeding the photocurrent density and low differential resistance values while maintaining maximum optical transparency. The lack of temperature stability of the TD parameters will affect the photoelectric parameters of the MJ PCs. Taking into account the results of previously performed modeling [2], in the temperature range from 25 °C to 80 °C, studies of the current-voltage characteristics of TDs based on two types of n^{++}-GaAs/p^{++}-$Al_{0.4}Ga_{0.6}As$ and n^{++}-GaAs/*i*-GaAs/p^{++}-$Al_{0.4}Ga_{0.6}As$ structures were carried out.

Materials and Methods

Using the molecular beam epitaxy (MBE) method, two types of TD structures were grown on *n*-type GaAs substrates (diameter 76.2 mm): A (see Table 1) and B (see Table 2). The structures are a tunnel n^{++}-GaAs/p^{++}-$Al_{0.4}Ga_{0.6}As$ heterojunction. Degenerate GaAs n^{++}-type δ-layers are doped with Si, and p^{++}-$Al_{0.4}Ga_{0.6}As$ layers are doped with C atoms. The doping levels of the n^{++} and p^{++} layers in the structures were, respectively, $\geq 1\cdot10^{19}$ cm^{-3} and ~ $1\cdot10^{20}$ cm^{-3}. The growth of heavily doped regions for both structures was carried out in identical modes at a substrate temperature of ~ 535–550 °C.

Table 1

Design of TD structure A

Layer type	Thickness, nm	$N_{A, D}$, cm^{-3}
p^+-GaAs:(C)	50	$2\cdot10^{19}$
p^+-$Al_{0.6}Ga_{0.4}As$:(C)	50	$1\cdot10^{19}$
p^{++}-$Al_{0.4}Ga_{0.6}As$:(C)	10	$1\cdot10^{20}$
n^{++}-GaAs:(δSi)	10	$\geq 1\cdot10^{19}$
n^+-$Al_{0.6}Ga_{0.4}As$:(δSi)	50	$4\cdot10^{18}$
n^+-GaAs:(Si)	200	$3\cdot10^{18}$
n^+-GaAs:(Si)	600000	$(1–3)\cdot10^{18}$

Table 2

Design of TD structure B

Layer type	Thickness, nm	$N_{A, D}$, cm^{-3}
p^+-GaAs:(C)	50	$2\cdot10^{19}$
p^+-$Al_{0.6}Ga_{0.4}As$:(C)	50	$1\cdot10^{19}$
p^{++}-$Al_{0.4}Ga_{0.6}As$:(C)	10	$1\cdot10^{20}$
i-GaAs	7	$\geq 5\cdot10^{14}$
n^{++}-GaAs:(δSi)	10	$\geq 1\cdot10^{19}$
n^+-$Al_{0.6}Ga_{0.4}As$:(δSi)	50	$4\cdot10^{18}$
n^+-GaAs:(Si)	200	$3\cdot10^{18}$
n^+-GaAs:(Si)	600000	$(1–3)\cdot10^{18}$

In comparison with structure A, in structure B an undoped *i*-GaAs layer with a thickness of ~ 7 nm was grown between degenerate n^{++}-GaAs:(δSi) and p^+-$Al_{0.6}Ga_{0.4}As$:(C) layers. The thickness of the *i*-layer was chosen taking into account the influence of temperature diffusion of the Si impurity during the subsequent growth of the monolithic structure of the MJ PCs [2]. The structures contained wide-gap n^+-$Al_{0.6}Ga_{0.4}As$:(δSi) and p^+-$Al_{0.6}Ga_{0.4}As$:(C) layers adjacent to the degenerate TD regions. These layers are necessary to prevent the temperature diffusion of dopant atoms from degenerate layers into the layers of photoactive sub-elements of the MJ PC. After completion of epitaxial growth of the grown heterostructures were annealing in an MBE chamber simulating the growth process of an MJ PC. The structures were annealed for 2 hours at a temperature of 580 °C at a pressure $p = 2\cdot10^{-7}$ Torr. TD chips with a mesa diameter of 225 μm were formed on the grown structures.

Results and Discussion

Directly on parts of structures A and B with manufactured TDs, current-voltage characteristics were measured in the temperature range from 25 °C to ~ 80 °C. The results are presented in Fig. 1, *a* (structure A) and Fig. 1, *b* (structure B), the current-voltage characteristics for structures without temperature annealing are indicated “before annealing”, and for structures after annealing – “after annealing”. The current-voltage characteristics were measured at a positive bias voltage of up to 0.6 V. It can be seen that the shape of the current-voltage characteristics of samples of structure A corresponds to a backward diode, which is explained by the insufficient level of degeneracy of the n^{++}-GaAs:(δSi) region [5]. The current-voltage characteristic does not show a section with a negative differential resistance, however, in the voltage range from 0 to 50 mV there is a quasi-linear section corresponding to band-to-band quantum tunneling.

In structure B, due to the presence of an undoped *i*-GaAs nanolayer between the degenerate *n* and *p* regions, a typical current-voltage characteristic of a TD (Esaki) is observed. Similar to structure A, the low Jp values for structure B compared to the results obtained earlier in [2] are due to an insufficient doping level of n^{++}-GaAs:(δSi) region (Table 1, 2), [2, 5].

The Fig. 2 illustrates the spread of J_p values for the quasi-linear section of the current-voltage characteristics of structure A and B. The type of structure is indicated on the abscissa axis, where A and B correspond to diodes without annealing, and “A anneal.” and “B anneal.” – diodes on annealed plate fragments. It can be seen that the maximum J_p value of the TD structure B is an order of magnitude higher compared to structure A. After annealing, the average J_p values for samples of both structures increased. Before annealing, the densities of the peak tunneling current in the quasi-linear section of structure A and the peak tunneling current of structure B are ~ 0.1 A/cm^2 and ~ 1 A/cm^2, and after annealing, ~ 0.15 A/cm^2 and ~ 1.5 A/cm^2, respectively. In addition, after annealing, the spread of J_p values increased, which may be due to uneven doping with carbon atoms and uneven diffusion of the Si impurity over the area of the epitaxial wafers due to the temperature gradient during the annealing process.

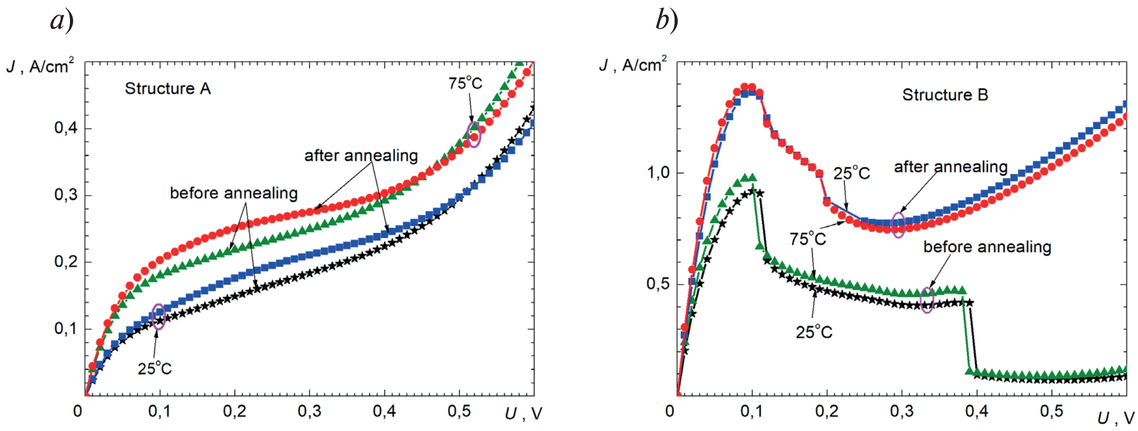

Fig. 1. Current-voltage characteristics of TD structures A-(*a*) and B-(*b*) at temperatures of 25 and 75 °C

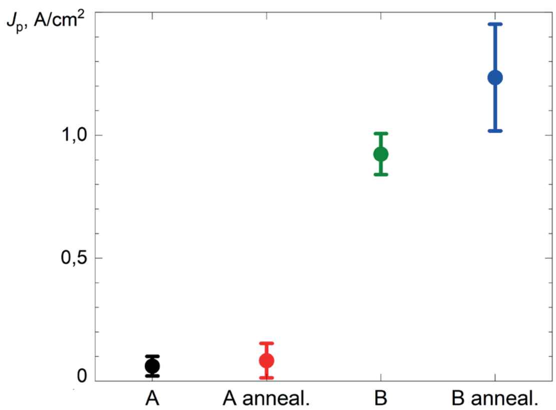

Fig. 2. Peak tunneling current density values for structures A and B before annealing (A, B) and after annealing (“A anneal.”, “B anneal.”)

From the current-voltage characteristics of TD structures A and B, measured in the temperature range (25–80) °C, the values of – J_p (Fig. 3, *a*) and differential resistance – R_d, which are responsible for parasitic losses when the voltage drops on the connecting TDs in MJ PCs, are calculated (Fig. 3, *b*). The temperature dependences of the calculated J_p и R_d parameters are presented in Fig. 3.

When heated from 25 to ~ 80 °C for structures A and B, an increase in J_p values is observed. This is due to a decrease in the band gap (E_g) of the semiconductor, a decrease in the height of the potential barrier, and an increase in the probability of quantum tunneling [6]. The best temperature stability of J_p is observed for TD samples of structure B (see Fig. 3, *a*), with the J_p value before annealing increasing by 6% and by 2% after annealing. For samples of structure A, the change in the maximum value of current density J_p is ~ 40%.

With an increase in the operating temperature of the TD from 25 to ~ 80 °C, a decrease in R_d values is observed for both structures. After annealing for TD structure B at T = 25 °C, R_d decreased by ~ 30% (from 67 mOhm·cm^2 to 46 mOhm·cm^2), and for structure A by ~ 6% (from 565 to 530 mOhm·cm2). For effective operation of the MJ PC, the connecting elements must provide the resistance of the linear section of the current-voltage characteristic at a forward bias voltage of less than 10 mOhm·cm^2 [4]. The increase in R_d can be due both to the diffusion of impurities and erosion of doping profiles, and to the presence of potential barriers created by isotype wide-gap n^+-$Al_{0.6}Ga_{0.4}As$:(δSi) and p^+-$Al_{0.6}Ga_{0.4}As$:(C) layers (Table 1 and 2), adjacent to the degenerate layers of the TD, which interfere with the transport of charge carriers [7]. The presence of the *i*-layer between the degenerate layers limits the interdiffusion of impurities and reduces the degradation of the current-voltage characteristics of the TD. The best temperature stability of R_d is observed for TD samples of structure B (see Fig. 3, *b*). When heated over the entire

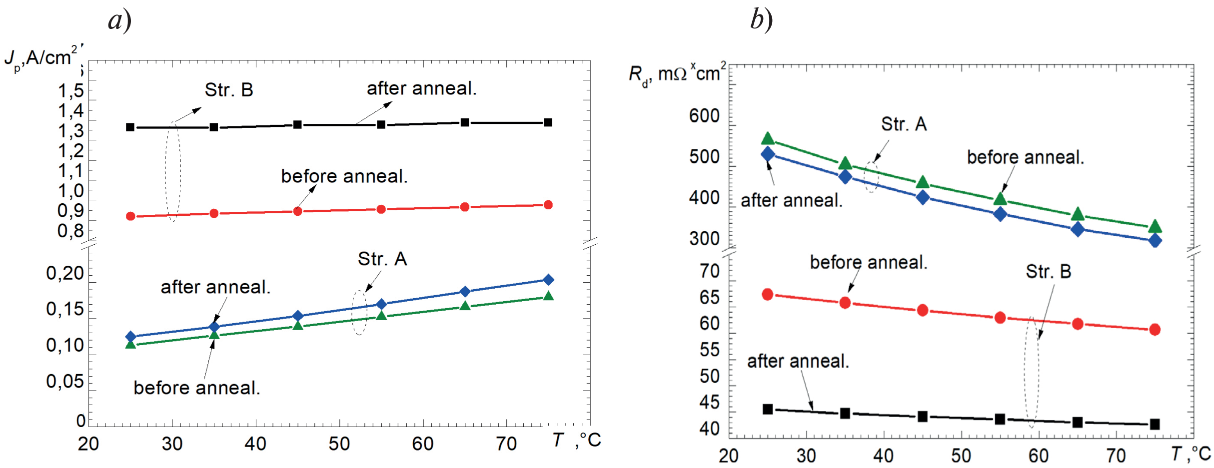

Fig. 3. Experimental temperature dependences of the parameters J_p (*a*) and R_d (*b*) for the samples of structures of types A and B before annealing and after annealing

temperature range, R_d for TD samples of structure B decreases by 9% from 67 to 61 mOhm·cm^2 before annealing and by 7% after annealing from 46 to 43 mOhm·cm^2. For structure A, upon heating, the R_d value changes by ~ 40% from 565 to 349 mOhm·cm^2 for TD samples before annealing and from 530 to 318 mOhm·cm^2 after annealing.

Conclusion

It has been experimentally demonstrated that the inclusion of a nanosized *i*-GaAs layer ($N_D \geq 5{\cdot}10^{14}$ cm^{-3}) between the degenerate n^{++}-GaAs:(δSi) (10nm) and p^{++}-$Al_{0.4}Ga_{0.6}As$:(C) (10 nm) regions of the connecting tunnel diode, even at a relatively low doping level of the n^{++}-layer, $N_D \geq 1{\cdot}10^{19}$ cm^{-3} ensures the presence of a tunneling current-voltage characteristic and promotes an increase in the peak tunneling current J_p by an order of magnitude compared to an identical structure, but without an *i*-GaAs layer. The results obtained are in qualitative agreement with the results of previously performed mathematical modeling of charge carrier transport in the proposed *p-i-n* structure of tunnel junction diodes. Tunnel diodes grown using molecular beam epitaxy n^{++}-GaAs:(δSi)/*i*-GaAs/p^{++}-$Al_{0.4}Ga_{0.6}As$:(C) provide an order of magnitude lower resistance values in the tunnel section of the current-voltage characteristic, higher temperature stability and maximum J_p values compared to the structure without *i*-layer. The proposed new design of the connecting TD provides good stability of characteristics under temperature influences corresponding to the regimes of epitaxial growth of monolithic MJ PC structures.

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Received 14.12.2023. Approved after reviewing 10.01.2024. Accepted 11.01.2024.