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TEMPERATURE CHARACTERIZATION OF GaAs/AlGaAs CONNECTING TUNNEL DIODES

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Abstract. The current-voltage characteristics of two types of GaAs-(δSi)/*i*-(GaAs/$Al_{0.2}Ga_{0.8}As$)/p^{++}-$Al_{0.2}Ga_{0.8}As$-(δBe) tunnel diode (TD) structures grown at different temperatures and epitaxial layer thicknesses have been investigated in the temperature range 100–400 K. Temperature dependences of the main TD parameters were determined: the peak value of the tunnel current density (J_p), the valley current density (J_v) and the differential resistance (R_d). TD samples of structure A grown at 500 °C exhibited the highest values of the peak current density ($J_p \leq 220$ A/cm^2) with temperature stability of 93 % over the whole temperature range. TD samples of structure B grown at 450 °C showed lower values of the peak tunneling current density ($J_p \leq 150$ A/cm^2), with significantly linear temperature dependence. Our findings can be used in the design and development of monolithic multijunction photoconverters of powerful laser radiation.

Keywords: current-voltage characteristics, tunnel diode, epitaxial layer, differential resistance, peak tunneling current

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ТЕМПЕРАТУРНАЯ ХАРАКТЕРИЗАЦИЯ СОЕДИНИТЕЛЬНЫХ ТУННЕЛЬНЫХ ДИОДОВ GaAs/AlGaAs

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Аннотация. В температурном диапазоне 400 – 100 K исследованы вольтамперные характеристики двух типов структур соединительных туннельных диодов (ТД) n^{++}-GaAs-(δSi)/*i*-(GaAs/$Al_{0,2}Ga_{0,8}As$)/p^{++}-$Al_{0,2}Ga_{0,8}As$-(δBe), отличающихся температурой роста и толщинами эпитаксиальных слоев. Определены температурные зависимости основных параметров ТД: пикового значения плотности туннельного тока J_p, плотности тока долины J_v и дифференциального сопротивления R_d. Образцы ТД структуры А, выращенной при температуре 500 °C, обеспечивают в диапазоне 100 – 400 K наибольшие значения пикового тока $J_p \leq 220$ А/см^2 при температурной стабильности величины около 93 %. ТД структуры В, выращенные при температуре 450 °C, показали меньшие значения плотности пикового туннельного тока: $J_p \leq 150$ А/см^2, с существенной линейной температурной зависимостью. Полученные результаты могут быть использованы при разработке и создании монолитных многопереходных фотопреобразователей мощного лазерного излучения.

Ключевые слова: вольтамперная характеристика, туннельный диод, эпитаксиальный слой, дифференциальное сопротивление, пиковый туннельный ток

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Introduction

High-power monolithic multijunction photovoltaic (PV) cells converting monochromatic light have potential for applications in optoelectronics systems operating both on Earth and in space. Such systems include a radiophoton phased array antenna array [1], energy-independent transceiver stations for free-space optical communication [2], batteries for autonomous optoelectronic devices, etc. [3, 4]. Depending on the optical power and the field of application, multijunction PV cells can operate in a wide temperature range (100–400 K) [5, 6]. Monolithic multijunction PV cells include several series-connected photoactive *p*–*n* junctions, i.e., semiconductor-based subunits with the same band gap width but with different geometries and doping levels of the layers. The subunits in the PV cell are connected via backward tunnel diodes (TD). The efficiency and reliability of multijunction PV cells significantly depends on the temperature stability of the parameters of the connecting TD: peak tunneling current density J_p, differential resistance R_d of the tunnel branch and high optical transparency over a wide range of operating temperatures. A distinct characteristic of connecting TD is the high degree of degeneration of sub-nanosized layers, achieved by the delta-doping method. However, interdiffusion of donor and acceptor impurities occurs in degenerate layers of TD during epitaxial growth of the entire structure of the PV cell, leading to profile smearing and a decrease in free charge carrier concentration. These factors have a significant impact on the parameters of the TD and the behavior of their temperature dependence.

In this paper, we experimentally measured the current–voltage (I–V) characteristics of GaAs/AlGaAs connecting tunnel diodes in the temperature range from 100 to 400 K, establishing the temperature dependences of the parameters J_p and R_d and analyzing the results obtained.

Experimental

Connecting p^{++}–i–n^{++} TD were considered for two types of structures: A and B, grown by molecular beam epitaxy (MBE). The distributions of atomic concentrations in the given structures, determined by secondary ion mass spectrometry (SIMS) are shown in Fig. 1. 'Quasi-neutral' i-regions were formed between the degenerate regions of both TD structures, consisting of two layers of different thicknesses: i-GaAs and i-$Al_{0.2}Ga_{0.8}As$. Both TD structures were grown on GaAs (100) p-type substrates with a beryllium concentration $N_A = 1 \cdot 10^{19}$ cm^{-3}. After the buffer layers were grown, the epitaxial temperatures were decreased to 500 and 450 °C for structures A and B, respectively.

A significant diffusion of the beryllium dopant into the degenerate region of n^{++}-GaAs doped with silicon was observed in both TD structures (see Fig. 1).

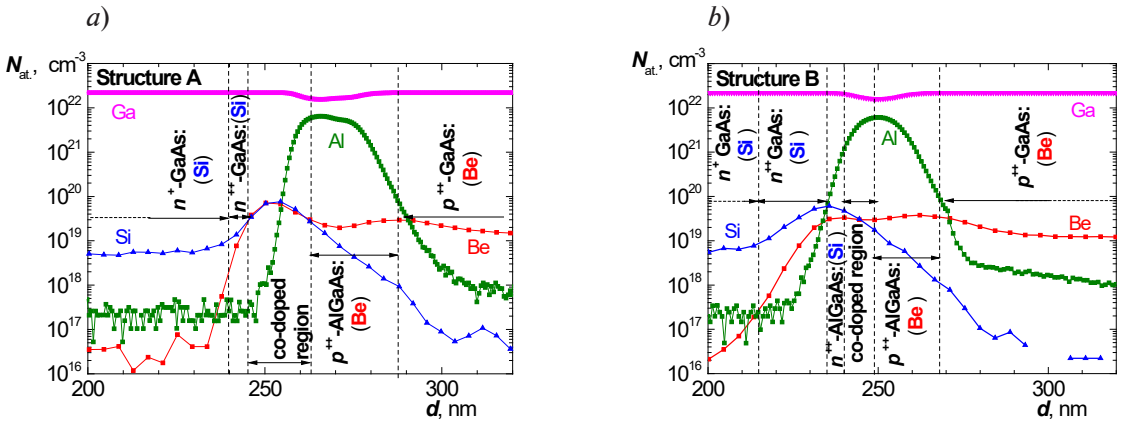

Fig. 1. Distribution of dopant concentration N_{at} over the thickness of the sample d in two types of TD structures: A (*a*) and B (*b*), determined by secondary ion mass spectrometry. Curves corresponding to different elements are shown in different colors

Analyzing the data in Fig. 1, we can conclude that diffusion of beryllium in structure A contributed to a decrease in the thickness of the n^{++}-GaAs and the concentration of free charge carriers in it, due to overcompensation of donor and acceptor impurities. The thickness of this layer, uncompensated by beryllium impurity, was approximately 5 nm with the concentration of silicon atoms varying from $1 \cdot 10^{19}$ to $3 \cdot 10^{19}$ cm^{-3} in structure A, and approximately 20 nm with the concentration varying from $9 \cdot 10^{18}$ to $6 \cdot 10^{19}$ cm^{-3} in structure B. Diffusion of beryllium atoms caused compensated quasi-neutral regions to appear between degenerate n^{++}- and p^{++}-layers. This is the co-doped region in Figs. 1,*a* and *b*. This region has a slightly larger thickness (about 25 nm) in structure A, consisting of two layers, GaAs:(Si, Be) and AlGaAs:(Si, Be) (see Fig. 1,*a*). This region consists of only one AlGaAs layer: (Si, Be) in structure B, with the thickness not exceeding 10 nm (see Fig. 1,*b*).

The measured peak concentrations of silicon and beryllium atoms approximately coincide in the overlap region of structure A, amounting to no more than $8 \cdot 10^{19}$ cm^{-3}. A different situation evolves in structure B, where the concentration of silicon atoms in the AlGaAs overlap region prevails over the concentration of beryllium atoms, with $N_D = 5 \cdot 10^{19}$ cm^{-3}, $N_A = 2 \cdot 10^{19}$ cm^{-3}.

Diode arrays with the mesa diameter of 225 μm, equipped with multilayer Ohmic contacts with n and p regions of AuGe-Ni-Au and AgMn-Ni-Au annealed in hydrogen at 500 °C, were formed on the TD structures by the post-growth technology.

I–V measurements of TD samples with structures A and B were performed at forward-bias voltages up to 1 V.

Results and discussion

Unlike structure B, structure A exhibited a spread in J_p values from 90 to 220 A/cm^2 at 300 K over an epitaxial wafer with a diameter of about 6 cm. The J_p values in the center of this wafer were close to the average of 116 A/cm^2, increasing to about 220 A/cm^2 at the periphery. A significantly smaller range of values, namely J_p = 125–150 A/cm^2, was obtained for samples in the center and at the periphery of the epitaxial wafer of structure B.

We selected TD samples from the central and peripheral regions of the epitaxial wafers of both structures to study the parameters J_p and R_d in the temperature range of 100–400 K. The I–V characteristics of the selected samples measured in the given range are shown in Fig. 2.

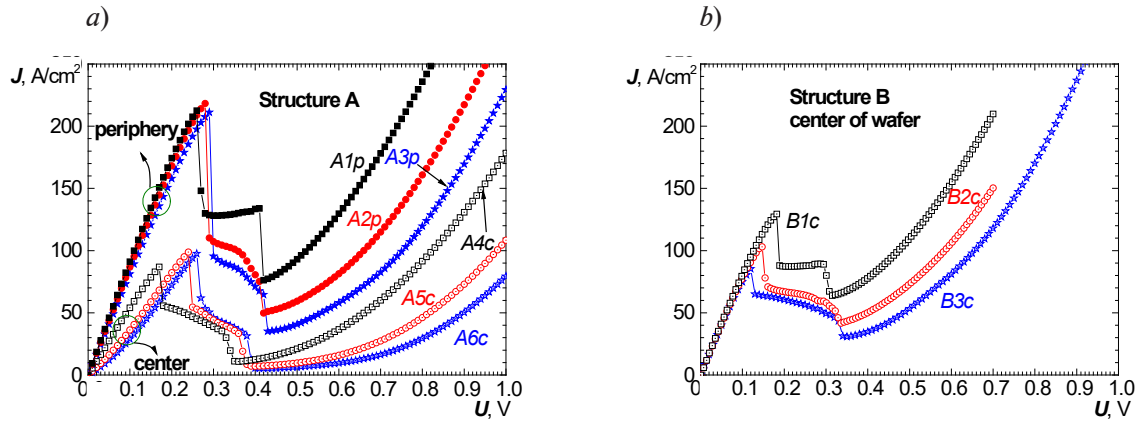

Fig. 2. Measurements of forward I–V characteristics in TD samples with two types of structures: A (*a*) and B (*b*) at different temperatures. Samples were taken at the periphery (curves *A1p*–*A3p*) and in the centers (*A4c*–*A6c*, *B1c*–*B3c*) of epitaxial wafers; *T*, K: 353 (*A1p*, *A4c*, *B1c*), 223 (*A2p*, *A5c*, *B2c*) and 123 (*A3p*, *A6c*, *B3c*)

Linear dependences are observed for the most part of the tunneling region in the experimental I–V curves obtained for any samples of structure B and peripheral structure A with a temperature decrease to 100 K (see Fig. 2). At the same time, an exponential dependence appears in the tunneling region of the I–V curves for samples from the center of structure A with a decrease in temperature. This behavior of dependences may be due to simultaneous influence of several factors.

As established in [7], the tunneling current in TD is determined by two transport mechanisms: interband quantum tunneling and trap-assisted tunneling. Both contribute to peak tunneling current density. The first mechanism is that electrons tunnel from occupied states of the conduction band to free states in the valence band through a potential barrier. The second, trap-assisted, transport mechanism, is due to the presence of localized impurity states (traps) in the band gap of the semiconductor. In this case, the tunneling electron is trapped, subsequently tunneling into the allowed states of the valence band. A decrease in temperature contributes to active freeze-out of charge carriers in traps; therefore, an increase in the electric field is required to overcome localized impurity states, leading to an exponential current-voltage dependence [8].

SIMS measurements for structure A (see Fig. 1,*a*) indicate that this transport mechanism may be predominant due to high degree of overlap of donor and acceptor impurities in the central region of the p^{++}–n^{++} tunnel junction.

We used the experimental data and expression (1) [9] to calculate the normalized temperature coefficient of the peak tunneling current density:

$$\Delta J_p = \frac{J_p^{T_j} - J_p^{T_{RT}}}{J_p^{T_{RT}}} \cdot 100\%, \qquad (1)$$

where ΔJ_p is the temperature coefficient; $J^{T_j}_p$, $J^{T_{RT}}_p$ are the peak tunneling current densities at fixed T_j and room temperature (T_{RT} = 300 K), respectively.

A positive value of ΔJ_p indicates an increase, and a negative value a decrease in the parameter J_p relative to its value at room temperature.

The dependences of J_p and ΔJ_p for structures A and B are shown in Fig. 3, *a*, *c*. TD samples from the central (*Ac* curves) and peripheral (*Ar* curves) parts of structure A exhibit higher thermal stability of peak tunneling current density, compared with samples from structure B (*Bc* curves). The variations in the maximum value of J_p amount to 17% for TD samples of structure A from the center and periphery of the wafer (*Ac* curve in Fig. 3,*a*) and 7% (*Ap* curve), respectively. The variation in the maximum value of J_p was 42% for TD samples of structure B (curve *Bc* in Fig. 3,*a*).

The parameter J_p decreases under heating from 300 to 400 K for TD samples taken from the center and periphery of the epitaxial wafer of structure A, with the value of ΔJ_p amounting to −9.5% in the center of the wafer and to −6.8% at the periphery(curves *Ac* and *Ap* in Fig. 3,*c*).

As the temperature decreased from 300 to 100 K, samples from the center of wafer A exhibited a nonlinear increase in the parameter J_p with the temperature coefficient $\Delta J_p = 7.5\%$, while the parameter J_p in peripheral samples decreased with the coefficient $\Delta J_p = -4.0\%$.

Notably, smooth maxima of peak tunneling currents are observed for the samples of structure A in Fig. 3,*a* in the temperature ranges of 150−250 K (*Ac* curve) and 200−300 K (*Ap* curve), respectively. The dependence of J_p for samples of structure B exhibits linear growth over the entire temperature range (curve *Bc* in Fig. 3,*a*). The value of ΔJ_p under heating from 300 to 400 K was 14%, and 29% under cooling to about 100 K.

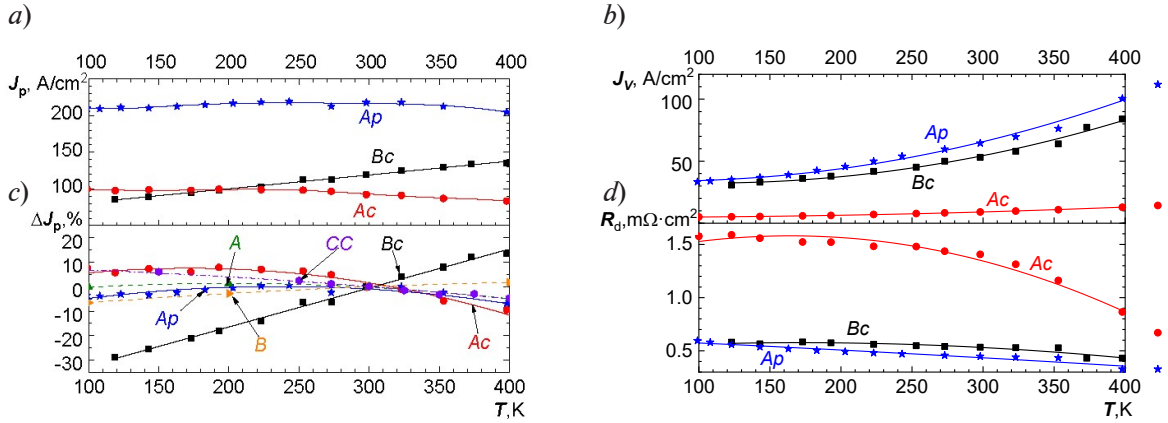

Fig. 3. Experimental (curves *Ac*, *Ap*, *Bc*) and calculated (*A*, *B*) temperature dependences for key parameters of TD samples of structures A and B: J_p (*a*), ΔJ_p (*c*), J_v (*b*), R_d (*d*). The samples were taken from the center (*Ac*, *Bc*) or from the periphery (*Ap*) of epitaxial wafers of structures A and B.
The calculated curve (*CC*) from [17] for a two-barrier resonant AlGaAs/GaAs tunnel diode is given for comparison

The behavior of the temperature dependence of J_p in TD samples with structures A and B depends on several factors with opposing influences on the value of J_p [6, 9]. Firstly, the band gap E_g of the semiconductor decreases with increasing temperature, leading to a decrease in the height of the potential barrier and an increase in the probability of quantum tunneling and the magnitude of J_p. Secondly, an increase in temperature reduces the degree of degeneracy of energy levels due to redistribution of electrons along them. The number of electrons in the conduction band at levels below the Fermi level E_F in the *n*-region E_c decreases, as some of the free electrons move to higher energy levels, and the Fermi level shifts downwards. As a result, the number of electrons capable of tunneling decreases, and the value of J_p decreases as well.

SIMS profiling (see Fig. 1) indicates that the doping level of the beryllium acceptor impurity in the degenerate p^{++}-AlGaAs region for both TD structures is approximately the same and is at least $2 \cdot 10^{19}$ cm^{-3}; in this case, the n^{++}-GaAs region has the predominant influence on the temperature characteristics of TD. As the concentration of free charge carriers decreases (below $1 \cdot 10^{19}$ cm^{-3}) in the n^{++}-GaAs region, the change in the position of the Fermi level starts to have the predominant

influence on the tunneling current J_p with an increase in temperature. The latter shifts closer to the bottom of the conduction band, and the value of J_p decreases. The change in the band gap has the predominant influence on the value of J_p in the range of 100–400 K at a higher concentration of free charge carriers (above $1 \cdot 10^{19}$ cm^{-3}), while the change in the position of the Fermi level has little effect; as a result, the value of J_p increases with increasing temperature.

We calculated the temperature dependences of ΔJ_p in TD similar to structures A and B (see Fig. 1) by the model described in [10]. The behavior of the calculated dependences of ΔJ_p (compare curves *A* and *B* in Fig. 3,*c*) is in qualitative agreement with the experimental ones (curves *Ac*, *Ar*, *Bc* in Fig. 3,*c*).

The presence of a negative temperature coefficient in the range of 300–400 K for the TD samples of structure A, in contrast to TD of structure B, indicates that the concentration level of free charge carriers of the n^{++}-GaAs region in the center and at the periphery of structure A is significantly lower than in structure B, due to the greater thickness of the overlap region and compensation of silicon and beryllium impurities (see Fig. 1,*a* and 2,*a*). Since the temperature coefficient of structure A from the center of the wafer is higher in absolute value for TD samples ($\Delta J_p = -9.5\%$) than for TD samples from the periphery ($\Delta J_p = -6.8\%$) at 400 K, the concentration of free charge carriers in the n^{++}-GaAs region of peripheral samples is slightly higher than in the center of the wafer with structure A but lower than in the center of the wafer with structure structure B. This is because the value of J_p increases for TD with structure B under heating with the temperature coefficient $\Delta J_p = 13.6\%$. The difference in parameters between the peripheral and central TD samples in the wafer of structure A may be due to a temperature gradient along the wafer even during the growth of the structure (the temperature at the periphery is several degrees lower than in the center). This leads to a decrease in the degree of overcompensation at the periphery.

The value of J_p of the TD considered is determined by the doping level and the degeneration degree of the n^{++}-GaAs TD layer. However, the J_p value in peripheral samples of TD with structure A is approximately 220 A/cm^2, while the corresponding maximum value for TD with structure B is about 150 A/cm^2. Our hypothesis is that this may be due to both the thickness of the 'quasi–neutral' overcompensated silicon-beryllium region [10] and the presence of a higher defect concentration in it due to overcompensation of impurity atoms [11–16]. This is also confirmed by the densities of valley currents in the dark *I–V* curves of the samples of the considered structures (see Figs. 2 and 3,*b*). As the forward bias voltage is increased (see Fig. 2), the current density first increases to the J_p value at a U_p voltage, and then decreases to the minimum value of the valley current density J_v at a U_v voltage due to a decrease in the degree of overlap of the conduction band with the valence band [9]. The valley current density is associated with the excess component of the current density of TD I–V characteristic. In turn, this excess component is determined by the concentration of deep levels inside the band gap of the semiconductor and the presence (or absence) of various types of structural defects. The defects contribute to dominance of an additional charge carrier transport mechanism associated with the resonant tunneling mechanism.

Since the overcompensation region is located between the degenerate n^{++} and p^{++} regions, it is depleted of the main charge carriers and is an 'effective' *i*-layer. We used numerical simulation [10] to establish that the dependence of J_p in tunnel diodes

$$n^{++}\text{-GaAs-}(\delta\text{Si})/i\text{-}(\text{GaAs/Al}_{0.2}\text{Ga}_{0.8}\text{As})/p^{++}\text{-Al}_{0.2}\text{Ga}_{0.8}\text{As-}(\delta\text{Be})\ (p\text{–}i\text{–}n)$$

on the thickness of the *i*-region is nonmonotonic. The peak current density first increases, reaching a maximum, and then decreases due to an increase in the thickness of the potential barrier through which the charge carriers tunnel.

Thus, the thickness of the 'effective' *i*-region caused by overcompensation of donor and acceptor impurities can affect the magnitude of J_p.

In addition, due to high concentration of silicon donors and beryllium acceptors, a higher concentration of defects and associated localized impurity states is present in the overcompensated 'effective' *i*-layer. Interband quantum tunneling acts as the main mechanism for transport of charge carriers in tunnel diodes with a sharp doping profile [11]. However, resonant tunneling (RT) begins to prevail in the presence of a sufficiently large region with overcompensation of donor and acceptor doping profiles and a high concentration of localized impurity states in the potential barrier [12]. In this case, resonance occurs if the energy of the states in the conduction

band coincides with the energies of the impurity states in the potential barrier and the allowed states in the valence band. The theory of RT through two localized impurity states is described in [13]. According to [14–16], localized states coinciding in energy and induced by a donor-acceptor pair contribute to a significant increase in J_p at low positive bias voltages in the TD. These assumptions are confirmed by the temperature dependence of J_p in resonant tunnel diodes.

For comparison, Fig. 3,*c* (*CC* curve) shows the temperature dependence of ΔJ_p for an AlGaAs/GaAs two-barrier resonant tunnel diode (RTD), simulated by the Hartree model, obtained in [17]. Analyzing this dependence, obtained under heating from 300 to 400 K, we can observe a decrease in the value of J_p at a negative temperature coefficient $\Delta J_p = -5\%$, the same as for structure A (see curves *Ac*, *Ap*). On the other hand, J_p increases smoothly under cooling from 300 to 100 K, giving the value of $\Delta J_p = 7\%$. The presence of a negative temperature coefficient in the I–V curves of RTD heated to 400 K is explained in [17] by scattering of charge carriers by phonons and electron-electron interaction.

We calculated the differential resistance responsible for parasitic losses at a voltage drop in TD in multijunction PV cells at different temperatures from the experimental I–V curves of the TD (Fig. 3,*d*). The connecting elements must provide resistances below 10 mOhm·cm^2 for effective operation of multijunction PV cells [6]. The dependences of differential resistance of the studied TD samples on temperature, accounting for resistance of the electrical circuit in the cryostat (about 0.7 mOhm·cm^2), are shown in Fig. 3,*d*. The best temperature stability R_d is observed for TD samples of structure B (see Fig. 3, *d*, curve *Bc*). The value of R_d varies from 0.58 to 0.42 mOhm·cm^2 over the entire temperature range for TD samples of structure B. The value of R_d varies from 1.59 to 0.67 mOhm·^{2} for TD samples from the central part and from 0.58 to 0.34 mOhm·cm^2 for samples from the peripheral part for structure A heated from 100 to 400 K.

The conducted temperature studies of forward I–V characteristics lead us to conclude that the developed connecting TD with structure A ensure the temperature stability of the parameters J_p, ΔJ_p at about 93% and the parameter R_d at about 59%, while structures B provide about 83% and 72%, respectively.

Conclusion

Forward current–voltage characteristics were studied for connecting tunnel diodes (TD) in the temperature range of 100–400 K, taking the form

$$n^{++}\text{-GaAs-}(\delta\text{Si})/i\text{-}(\text{GaAs}/\text{Al}_{0.2}\text{Ga}_{0.8}\text{As})/p^{++}\text{-Al}_{0.2}\text{Ga}_{0.8}\text{As-}(\delta\text{Be})$$

for two types of structures obtained by molecular beam epitaxy. The type A structure contained an overcompensated 'effective' *i*-layer with a thickness of ≤ 25 nm, formed by interdiffusion of silicon and beryllium at an epitaxial growth temperature of 500 °C. The type B structure had an 'effective' *i*-layer with a thickness of ≤ 10 nm, formed similarly at a growth temperature of 450 °C.

We observed a smooth decrease in the tunneling current density J_p for the TD with the structure A under heating to 400 K, while a linear growth of J_p was characteristic for the structure B. The change in J_p was 7% for TD samples with the structure A, and 42% for TD samples with the structure B. This J_p dependence on temperature for structure A is associated with the influence of temperature diffusion of the predominantly acceptor beryllium impurity from the layer

$$p^{++}\text{-Al}_{0.2}\text{Ga}_{0.8}\text{As-}(\delta\text{Be})$$

to the region

$$n^{++}\text{-GaAs-}(\delta\text{Si})/i\text{-}(\text{GaAs}/\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}).$$

This diffusion contributed to a decrease in the degeneracy of the n^{++}-GaAs-(δSi) layer of the TD due to formation of an overcompensated silicon and beryllium region.

The linear increase in J_p with an increase in temperature for structure B is due to a lower thickness of the 'effective' *i*-layer, a smaller diffusion depth of beryllium impurity into the n^{++}-GaAs region and, accordingly, the higher doping and degeneracy levels of this region.

The maximum values of J_p obtained in the temperature range of 100–400 K were about 220 A/cm^2 for structure A and about 150 A/cm^2 for structure B. Such values of J_p can be due to both the thickness of the 'effective' *i*-layer and by the level of localized impurity states initiating resonant tunneling.

Analyzing the measured I–V characteristics, we found that the differential resistances for TD samples of structure A lie within R_d = 0.58–0.34 mΩ·cm^2 in the temperature range from 100 to 400 K, and within 0.58–0.42 mΩ·cm^2 for structure B.

The TD samples collected at the periphery of the epitaxial wafer of structure A grown at 500 °C exhibit higher temperature stability and maximum values of J_p at minimum values of R_d. A high degree of overcompensation of doping impurities in the active region of the TD located in the center of the wafer leads to a decrease in the peak tunneling current density. Samples of structure B grown at 450 °C provide better stability of the peak current density across the wafer, but with a lower maximum value of J_p and worse temperature stability. We assume that the optimal conditions for growth of the TD structure of type

$$n^{++}\text{-GaAs-}(\delta\text{Si})/i\text{-}(\text{GaAs}/\text{Al}_{0.2}\text{Ga}_{0.8}\text{As})/p^{++}\text{-Al}_{0.2}\text{Ga}_{0.8}\text{As-}(\delta\text{Be})$$

with the maximum values of J_p, minimum values of R_d and high temperature stability lie in the epitaxial growth temperature range of $450 < T < 500$ °C.

The temperature diffusion of impurities in highly doped layers of connecting TD must be taken into account in designs of multijunction photovoltaic cells converting high-power optical radiation Including an undoped *i*-layer up to 10 nm thick between the highly doped TD layers as well as optimizing the epitaxial growth temperature can prevent parasitic diffusion of the impurity. Furthermore, it is important to use a dopant with a lower diffusion coefficient, for example carbon as an acceptor impurity.

We should note that taking into account the contribution of resonant tunneling in connecting TD with high optical transparency has potential for constructing highly efficient multijunction photovoltaic converters of high-power laser radiation.

SIMS studies were performed using the equipment of the Center for Collective Use “Materials Science and Diagnostics in Advanced Technologies” (Ioffe Institute).

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