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Modeling of a capacitive MEMS switch with "floating" electrode

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Abstract. Primary characteristic of a capacitive MEMS switch is the ratio of capacitances in the open and closed states. Conventional switches have this ratio from several units to several tens. However, it can be significantly increased by mounting a "floating" electrode onto the transmission line. The analytical approach provides the capacitance ratio of the modified switch as high as 10^5. Finite element simulation takes parasitic capacitance into account and gives significantly lower value. In this work, the dependence of capacitive characteristics and S-parameters on the substrate properties is investigated. The ways for enhancing the switch performance are proposed.

Keywords: MEMS switch, capacitance ratio, floating potential, finite element method

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Моделирование емкостного МЭМС-переключателя с «плавающим» электродом

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Аннотация. Основной характеристикой емкостного МЭМС-переключателя является отношение емкостей в разомкнутом и замкнутом состояниях. Для стандартных изделий это отношение составляет от нескольких единиц до нескольких десятков. Однако его можно значительно увеличить, используя «плавающий» электрод на линии передач. Согласно аналитическим расчетам, отношение емкостей модифицированного переключателя составляет около 10^5. Моделирование методом конечных элементов учитывает паразитную емкость и дает существенно меньшее значение. В настоящей работе исследована зависимость емкостных характеристик ключа и S-параметров от свойств подложки и предложены способы их улучшения.

Ключевые слова: МЭМС-переключатель, отношение емкостей, плавающий потенциал, метод конечных элементов

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Introduction

MEMS switch is an electromechanical relay of micron size fabricated by microelectronic techniques [1, 2]. It provides low insertion loss and high isolation in combination with small dimensions and virtually zero power consumption [3]. These features make MEMS switches attractive for advanced communication systems, radar equipment and other areas of radio electronics [4]. The recent growth of wireless communications and increased demands driven by 5G standard (high cutoff frequencies, small space availability in mobile phones and battery-operated devices) offer wide opportunities for MEMS switches. Many applications require switches with capacitive contact that ensure wider bandwidth in comparison with resistive devices. An important parameter of this switch is the ratio of capacitances in the open and closed states C_{on}/C_{off} [5]. In conventional devices, this ratio varies from several units to several tens in the best case [6, 7]. Implementation of novel design solutions significantly improves C_{on}/C_{off}. This work is devoted to the MEMS switch equipped by a "floating" electrode.

Materials and Methods

The proposed switch is schematically shown in Fig. 1, *a*. A movable electrode is an aluminum beam with a length of 100 μm, which is fixed on torsion suspensions. A transmission line runs under the beam at a distance of 1 μm. A thin metal electrode is formed on top of the dielectric layer. In the open state, the potential of the electrode is floating. The capacity of the beam-line system is small, so the signal passes from the input to the output with minimal losses. In the closed state, the beam touches the electrode, and their potentials are equalized. The capacity between the beam and the line increases significantly, so the switch shunts the line. The signal does not pass from the input to the output, and high isolation is achieved. The concept of the "floating" electrode is thoroughly described in our previous work [8]. Driving electrodes are located under both arms of the beam, so an additional restoring force may be applied in case of stiction. This design significantly improves the reliability of the switch compared to the classical one-electrode structure.

The switch is simulated by the finite element method (FEM) [9]. The model includes a chip with a coplanar transmission line and contact pads, as shown in Fig. 1, *b*. The line consists of a 100 nm thick ruthenium layer covered by 1 μm thick aluminum metallization and has a characteristic impedance of 50 Ohm. It is formed on a 460 μm thick substrate covered by silicon dioxide layer with a thickness of 1 μm. The switch is built into one of the grounded conductors, as shown in Fig. 1, *c*. A test signal with the amplitude of 1 V and frequency of 300 kHz is applied to the central conductor from a power supply with a resistance of 50 Ohm. The capacitance is calculated using the total energy of the electric field. S-parameters are calculated by analyzing the transverse electro-magnetic wave applied to the contact pad.

Results and Discussion

In the open state, the switch is equivalent to series-connected capacitors. The first capacitor is formed by the transmission line and the "floating" electrode, while the second one consists of the electrode and the beam. The second capacitance is significantly lower than the first one. Therefore, it determines total capacitance in the open state:

$$C_{off} = \varepsilon_0 \frac{S}{g-d} = 0.4 \cdot 10^{-3}\ pF, \tag{1}$$

where S = 50 μm² is the overlap area of the beam with the electrode; g = 1 μm is the gap between them; d = 50 nm is the thickness of the dielectric layer, ε_0 is the dielectric constant.

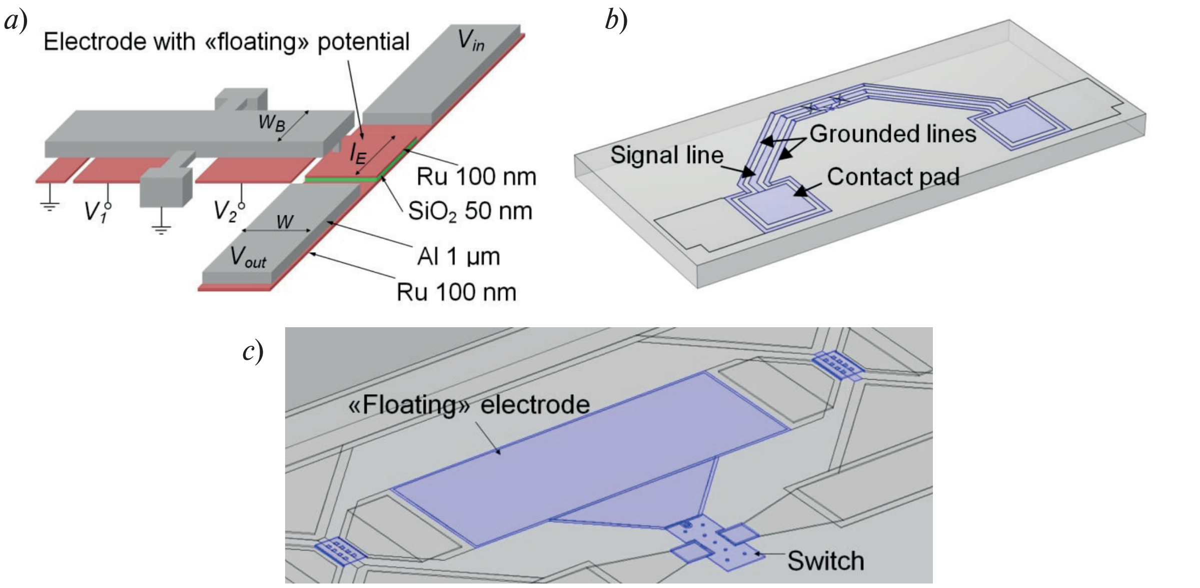

Fig. 1. A switch with “floating” electrode: schematic illustration (*a*); a model of the chip (*b*); a close-up view of the beam and electrode (*c*)

In the closed state, the second capacitor is converted to a contact resistance, so the total capacitance is determined by the first capacitor:

$$C_{on} = \varepsilon_0 \varepsilon \frac{l_E w}{d} = 39.75\ pF, \tag{2}$$

where l_E = 394 μm is the length of the “floating” electrode; w = 150 μm is the width of the line; ε = 3.8 is the dielectric permittivity of silicon dioxide. Thus, the switch has a capacitance ratio of 10^5, which is an order of magnitude higher than C_{on}/C_{off} for most conventional devices.

Expressions (1) and (2) do not take into account the parasitic capacitance. FEM simulation considers real configuration of the transmission line and substrate properties. The dependence of capacitive properties on the resistivity ρ of the silicon wafer is shown in Fig. 2, *a*. Increasing ρ reduces both C_{on} and C_{off} due to a decrease in the parasitic component. In turn, the drop of C_{off} increases the capacitance ratio. The maximum value is 7.4 at ρ = 50 kOhm·cm, which is significantly lower than the analytical prediction. The reason for the discrepancy is the relatively large C_{off} = 7.4 pF.

The coplanar line is schematically shown in Fig. 2, *b*. Its capacitance can be calculated by the method of conformal mapping [10]. The off-state value is determined as follows:

$$C_{off} = C_{air} + C_{sub} = 2\varepsilon_0 \left(\frac{K(k_1)}{K(\tilde{k}_1)} + \frac{K(k_0)}{K(\tilde{k}_0)} \right) + 2\left|\varepsilon_{r2} - \varepsilon_{r1}\right| \varepsilon_0 \frac{K(k_2)}{K(\tilde{k}_2)}, \tag{3}$$

where C_{air} and C_{sub} are the capacitances of air and substrate regions, ε_{r2} and ε_{r1} are the dielectric permittivity of silicon dioxide and the substrate, $K(k)$ is the complete Legendre elliptic integral of the first kind:

$$K(k_i) = \int_0^1 \frac{1}{(1-x^2)(1-k_i^2 x^2)} dx, \tag{4}$$

and the moduli k_i, $\tilde{k}_i$ are described as:

$$k_i = \frac{\tanh\left(\dfrac{\pi \cdot w}{4 \cdot H_i} \right)}{\tanh\left(\dfrac{\pi \cdot (w + 2 \cdot a)}{4 \cdot H_i} \right)} \quad i = 0,1,2; \tag{5}$$

$$\tilde{k}_i = \sqrt{1 - k_i^2}. \tag{6}$$

According to equation (3), C_{off} can be reduced by using substrates with the dielectric permittivity close to that for SiO_2. This statement is confirmed by simulation results given in Table. Two dielectric substrates are considered, including sapphire and borosilicate glass Borofloat 33. The highest capacitance ratio of 46.1 is provided by Borofloat 33. The widely used sapphire wafer ensures almost two times lower value due to relatively high ε. A further increase in C_{on}/C_{off} requires changing the dimensions of the coplanar line, including the reduction of the width w of the central conductor and increasing the distance a between the conductors.

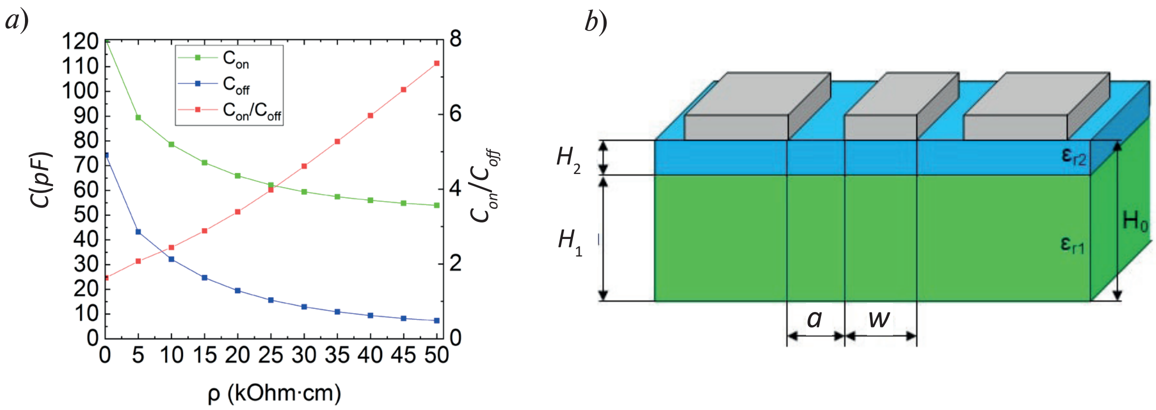

Fig. 2. Dependence of the switch characteristics on the resistivity of the substrate (*a*) and schematic illustration of a coplanar line on a double-layer dielectric substrate (*b*)

Table

Simulated capacitive characteristics for various substrates

Material	ε	ρ, Ohm·cm	C_{on}, pF	C_{off}, pF	C_{on}/C_{off}
Low-resistivity Si	11.7	12	120.9	74.2	1.6
High-resistivity Si	11.7	$5{\cdot}10^3$	89.4	43.2	2.1
Sapphire	9.3	10^{16}	48.4	1.8	27.7
Borofloat 33	4.6	10^8	47.7	1.0	46.1

The next step is the estimation of insertion loss and isolation. Insertion loss is the amount of signal attenuation between the input and output ports when the switch is in the "on" state (the beam is in the upper position). Expressed in decibels, insertion loss must be close to zero for maximum power transfer. Isolation is the amount of signal attenuation between the input and output ports in the "off" state (the beam touches the floating electrode). This value has to be as large as possible. FEM simulation is carried out for four substrates indicated in Table.

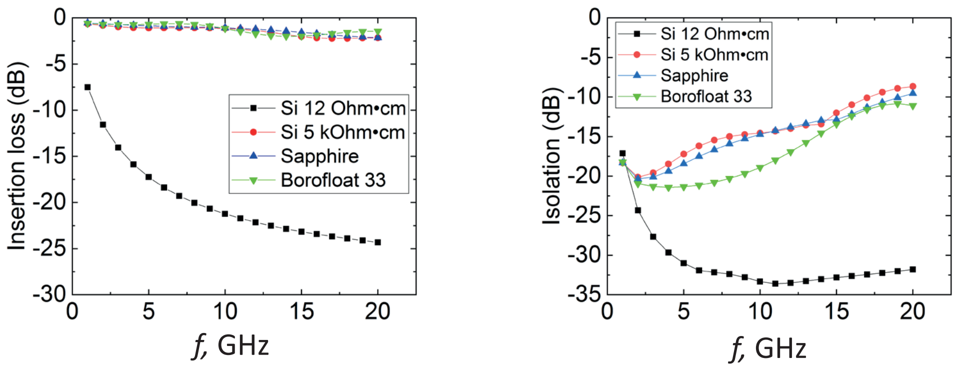

Fig. 3. Insertion loss (*a*) and isolation (*b*) for the silicon and sapphire substrates

The results are shown in Fig. 3. Low-resistivity Si provides high insertion loss in the range from -10 dB to -30 dB over the entire frequency range. The situation is much better for the high-resistivity Si, which ensures the loss higher than -3 dB for the entire frequency range, as well as for dielectric substrates. These materials also provide better isolation than high-resistivity Si. Borofloat 33 substrate is the best choice for our switch, which has better isolation, low insertion loss and acceptable capacitance ratio of 46.1.

Conclusion

The paper describes theoretical analysis of the capacitive MEMS switch with a floating electrode. Working characteristics are calculated analytically and by a finite element method. The switch can provide a capacitance ratio as high as 10^5, but the parasitic capacitance should be rather low. To reduce the parasitic component, one has to increase the substrate resistivity. Dielectric substrates ensure more than 10 times higher C_{on}/C_{off} compared to silicon. A commonly used Borofloat 33 provides excellent insulation and acceptable insertion loss in the entire frequency range. However, even with the glass substrate the capacitance ratio does not exceed 46.1. This value can be further increased by optimizing the size of the transmission line.

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