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Simulation and analysis of heterostructures for normally-off p-channel GaN transistor

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Abstract. This article presents the results of simulation the heterostructure of normally-off p-channel transistor. The design of the upper layers of the heterostructure was determined to induce the appearance of a 2DHG at the p-GaN/AlGaN heterojunction. By studying the band diagrams, the dependence of the transistor behavior on the thickness of the p-GaN and the impurity concentration within it is demonstrated for the p-channel device. Additionally, through analysis of the current-voltage characteristics the relationship between the formation of a normally-on or normally-off transistor and the thickness of the p-GaN layer, as well as the impurity concentration within it, was determined.

Keywords: heterostructure, power transistor, p-channel, p-GaN, AlGaN

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Моделирование и анализ гетероструктур для нормально закрытого p-канального GaN-транзистора

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Аннотация. В данной работе представлены результаты моделирования гетероструктуры для создания нормально закрытого p-канального транзистора. Конструкция верхних слоев гетероструктуры определялась условием возникновения двумерного дырочного газа (2DHG) на гетеропереходе p-GaN/AlGaN. Исследование зонных диаграмм продемонстрировало зависимость поведения транзистора от толщины слоя p-GaN и концентрации примесей в нем. Обнаружена зависимость формирования нормально открытого или нормально закрытого транзистора от толщины p-GaN и концентрации в нем примесей.

Ключевые слова: гетероструктура, мощный транзистор, p-канал, p-GaN, AlGaN

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Introduction

P-channel GaN power transistors offer distinct advantages over their n-channel GaN counterparts, making them valuable in various applications. They can be integrated with n-channel transistors on the same chip to form complementary pairs, enabling higher voltage operation and improved gain coefficients compared to devices solely relying on n-channel GaN transistors. P-channel GaN power transistors find utility in inverters, DC-DC converters, AC-DC converters, and power supplies. Nonetheless, similar to any emerging technology, p-channel GaN power transistors encounter limitations and challenges. Notably, they exhibit higher production costs compared to traditional silicon-based power transistors, and their reliability is currently constrained. However, ongoing advancements in production techniques and dedicated research in this field are expected to enhance the prevalence and competitiveness of p-channel GaN power transistors in power electronics [1].

The exploration of novel heterostructures capable of facilitating the development of p-channel devices has yielded successful outcomes in the form of logic circuits utilizing complementary pairs based on GaN, comprising both p-channel and n-channel transistors [2, 3]. These papers delve into the investigation of p-channel GaN-based HFETs (Heterojunction Field Effect Transistors), highlighting their potential for achieving high breakdown voltage and low leakage on a single wafer. By optimizing the heterostructure upon which the transistor is fabricated, it becomes feasible to create a p-GaN transistor with a breakdown voltage surpassing 1000 V [4]. Key factors influencing the transistor's performance include the thickness and composition of the channel and barrier layers.

One approach to realize normally-off p-channel power transistors involves utilizing metal-oxide-semiconductor field-effect transistors (MOSFETs), wherein an aluminum oxide-based dielectric and magnesium doping of GaN are employed. However, to ensure high performance and reliability in practical applications, it is essential to consider the intricacies of modeling GaN transistors within TCAD simulators (Technology Computer-Aided Design) [5]. The modeling of GaN-based power transistors in TCAD is an active area of research, wherein the advent of new technologies and materials contributes to improving result accuracy and expanding the range of applications for GaN transistors across various fields.

In this study, our objective was to simulate a heterostructure with the aim of creating a normally-off p-channel transistor. We examined the influence of specific device parameters, namely the doping of the p-GaN layer and its thickness. The design of the upper layers of the heterostructure was guided by the condition necessary for the emergence of a two-dimensional hole gas (2DHG) at the p-GaN/AlGaN heterojunction. We investigated the potential for forming both normally-on and normally-off transistors within this framework.

Materials and Methods

The main goal in solving the problem of choosing the design of a normally-off transistor is to study the dependence of the charge carrier concentration in the channel on the structure parameters. The design of the heterostructure layers is shown in Fig. 1. It consisted of a 3.5 um $Al_{0.05}Ga_{0.95}N$ buffer layer, a 15 nm $Al_{0.2}Ga_{0.8}N$ barrier layer, and a Mg-doped p-type GaN layer with variable thickness. To form a gate dielectric in a p-channel transistor, a 20 nm layer of aluminum oxide was applied to the heterostructure surface. The presence of a thick buffer layer aims to ensure a high breakdown voltage.

This heterostructure is ideal for creating n- and p-channel transistors on the surface of the same silicon substrate. The $Al_{0.2}Ga_{0.8}N$/ $Al_{0.05}Ga_{0.95}N$ heterojunction facilitates the formation of a two-dimensional electron gas (2DEG), enabling the construction of an n-channel transistor (located on the right side of Fig. 1). Simultaneously, the heterointerface between p-GaN and

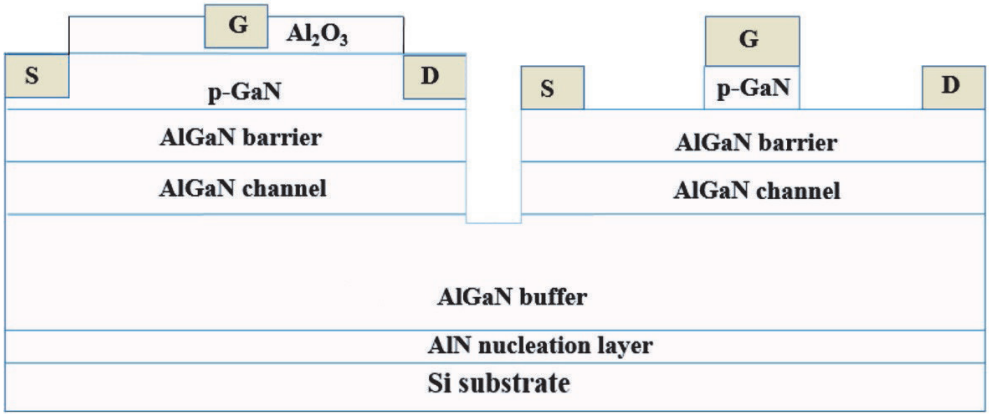

Fig. 1. Schematic cross-sectional view of a p-channel HFET (left side) and an n-channel HFET (right side) on the same wafer

$Al_{0.2}Ga_{0.8}N$ generates a two-dimensional hole gas (2DHG), which can be utilized to construct a p-channel transistor (located on the left side of Fig. 1).

Later, in the chosen heterostructure, we focused only on the p-GaN/$Al_{0.2}Ga_{0.8}N$ heterojunction.

Modeling has been done with Sentaurus Technology Computer Aided Design (TCAD). Sentaurus TCAD contains several physical models that describe the physics of the device most closely to reality (spontaneous and piezoelectric polarization, drift-diffusion model, thermodynamic model).

The level of doping of GaN layer with magnesium and the level of carrier concentration in the p-channel layer of GaN-based transistor have a relationship. Due to the polarization characteristic of nitrides of the third group, 2DHG is formed at the boundary of the p-GaN/AlGaN heterojunction in the absence of voltage at the gate. Doping the GaN layer with magnesium allows to introduce additional impurity magnesium atoms into the semiconductor matrix, which in turn increases the concentration of charge carriers in the p-channel layer of the transistor.

Initially, for the p-GaN layer, the conditions for the onset of the appearance of a two-dimensional hole gas were determined when the concentration of the magnesium dopant was changed from 1 to $50 \cdot 10^{18}$ cm^{-3}. Band diagrams were simulated and the p-GaN/$Al_{0.2}Ga_{0.8}N$ heterojunction was considered.

The presence of a two-dimensional hole gas was detected by a spike in the hole concentration at the heterojunction as a result of band bending and the crossing of the Fermi level by the valence band. In this case, the states were simulated with an applied voltage to the transistor gate from 0 V to 3 V. In the absence of voltage at the gate in a normally-off transistor, the concentration of charge carriers should tend to zero, and when voltage is applied, it should increase sharply, indicating the passage of current. Then these calculations were carried out for all thicknesses in the range from 10 to 80 nm.

According to the data obtained as a result of the simulation, the state of the future transistor was found: normally-on or normally-off. For a structure corresponding to a normally-off transistor, the current-voltage characteristics of the transistor were modeled at various values of the gate voltage.

Results and Discussion

In the absence of gate voltage, the appearance of a two-dimensional hole gas at a p-GaN/$Al_{0.2}Ga_{0.8}N$ heterojunction with a p-GaN thickness of 100 nm occurs at a doping dose of about $8 \cdot 10^{18}$ cm^{-3}. The band diagram with the presence of 2DHG is shown in Fig. 2, *a*. As can be seen from the figure, the valence band E_v at the heterojunction bends and tends to cross the Fermi level E_{fp}. In this case, a high concentration of holes N_h arises in this region, which reaches 10^{19} cm^{-3}. The conduction band E_c is far enough away from the fermi level, applying the negative gate voltage required to open the p-channel transistor does not result in other charge carriers (electrons).

At lower dopant concentrations, no two-dimensional gas is formed. As shown in Fig. 2, *b*, at a lower impurity concentration in gallium nitride and in the absence of voltage at the gate electrode, the hole concentration N_h tends to zero. This is due to the fact that the valence band E_v is farther from the Fermi level E_{fp}, and its bend towards the Fermi level E_{fp} is less pronounced.

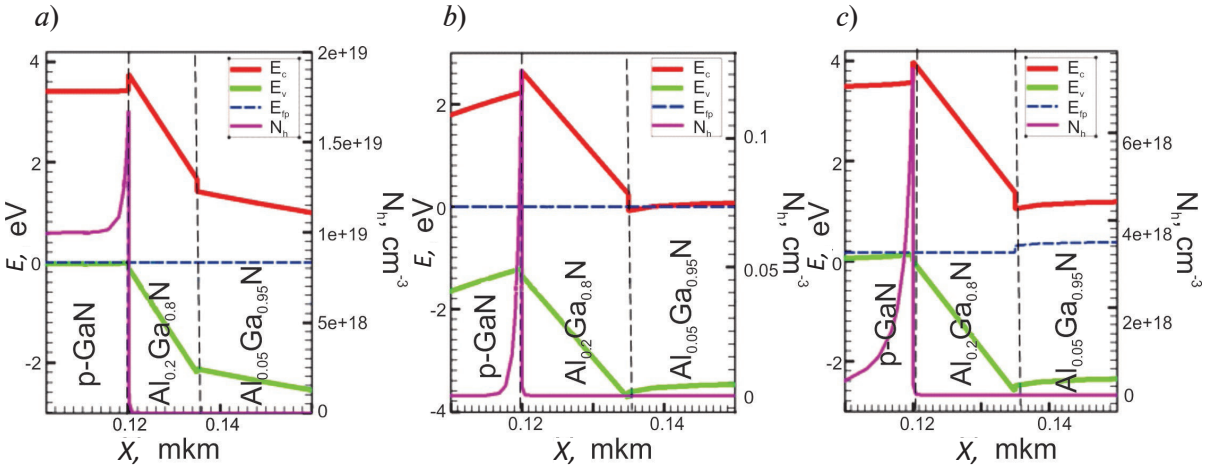

Fig. 2. Band diagram of a p-channel GaN transistor: too high density of holes in the channel in the absence of voltage on the gate $V_g = 0$, the device is essentially normally-on (*a*); low hole density in the channel by $V_g = 0$ (*b*); $V_g = 3$, the transistor is open and the density of holes in the channel has increased dramatically (*c*)

When a voltage of 3 V is applied to the gate, the valence band E_v at the heterojunction begins to strongly bend and crosses the Fermi level E_{fp}. Consequently, a substantial concentration of holes N_h emerges in this region, reaching $7 \cdot 10^{18}$ cm^{-3}. This behavior is illustrated in Fig. 2, *c*, which demonstrates the opening of the channel when the gate voltage is applied.

Lowering the dopant concentration in the p-GaN cap layer can have a positive impact on the quality of the GaN material. This decrease can result in an increase in the surface potential, leading to a higher threshold voltage for the transistor and improved key characteristics. However, selecting the optimal doping level for the p-GaN layer is crucial since the impurity concentration has a complex effect on the transconductance and drain current, which are important for both digital and analog applications.

After determining the type of transistor, the thickness of the p-GaN layer was varied to identify the conditions for normally-off operation. Fig. 3 illustrates the relationship between the on and off regimes in terms of dopant concentration N_p and p-GaN layer thickness $h_{\text{p-GaN}}$. It is evident that when modifying the design of a normally-off transistor, a decrease in $h_{\text{p-GaN}}$ thickness should be accompanied by an increase in N_p doping value, and vice versa. Points located above the curve in the figure correspond to a normally-on p-channel transistor, while points below the curve correspond to a normally-off one.

Based on the optimal design parameters of a normally-off p-channel transistor ($h_{\text{GaN}} = 50$ nm, $N_p = 1 \cdot 10^{19}$ cm^{-3}) the output parameters of the transistor were simulated. As a result of simulations at a drain-source voltage $V_{DS} = -20$ V the transistor showed a current of about 0.8 mA/mm at a gate voltage of $V_G = 12$ V.

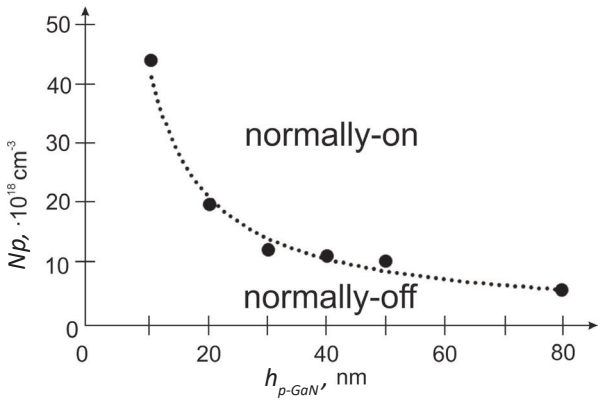

Fig. 3. Dependence of type p-channel device on p-GaN thickness and its activated impurity concentration

Conclusion

Simulation of normally-off p-channel p-GaN/$Al_{0.2}Ga_{0.8}N$/$Al_{0.05}Ga_{0.95}N$/AlN/Si HFET (heterostructure field-effect transistor) based on a p-GaN was demonstrated. The conditions for the formation of two-dimensional hole gas were found. Using Sentaurus TCAD, the effect of heterostructure parameters on the device behaviour was investigated. On the basis of these studies the optimal composition of the heterostructure for obtaining a normally-off transistor: p^+-GaN with a gate thickness of 50 nm and impurity concentration 1×10^{19} cm^{-3}, $Al_{0.2}Ga_{0.8}N$ with a thickness of 15 nm, $Al_{0.05}Ga_{0.95}N$ with a thickness of about 3500 nm. The threshold voltage of the obtained structure is of the order of 3 V. Reducing the dopant concentration in the p-GaN layer while the structure remains within the limits of the normally-off transistor conditions can positively affect on the quality of the GaN material. Thus, it is possible to contribute to an increase in the surface potential, and to form a higher threshold voltage for the transistor and improve the performance of the switch. The results show that p-channel GaN HFETs are viable candidates for high-voltage switching devices and their gate drivers.

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