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Development of detector cluster based on silicon photomultipliers for the Cherenkov gamma-ray telescope TAIGA-IACT

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Abstract. A new experimental detector cluster for the TAIGA-IACT telescope has been developed. The cluster contains 28 pixels based on MicroFJ-60035 silicon photomultipliers, whose signal is digitized with an analog memory chip (switched capacitor array) DRS4 at a frequency of up to 5 GHz. The paper describes the device and the operation principles of the detector cluster, reveals the peculiarities encountered in the development process. Dark chamber tests of the cluster with a point source of short pulses of ultraviolet light have allowed us to obtain dependencies of the cluster conversion coefficient and the maximum value of the recorded signal on the overvoltage of the silicon detectors.

Keywords: SiPM, silicon photomultipliers, readout electronics, IACT

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Разработка детекторного кластера на кремниевых фотоумножителях для черенковского гамма-телескопа TAIGA-IACT

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Аннотация. Создан новый экспериментальный детекторный кластер для телескопа TAIGA-IACT. Кластер содержит 28 пикселей с кремниевыми фотоумножителями MicroFJ-60035, сигнал с которых оцифровывается с применением микросхемы аналоговой памяти DRS4 с частотой до 5 GHz. В работе описывается устройство и принцип работы детекторного кластера, раскрываются сложности, с которыми пришлось столкнуться в процессе разработки. Также в работе описывается проведение испытаний в темной камере с точечным источником коротких импульсов ультрафиолетового света, в результате которых были получены зависимости коэффициента преобразования кластера и максимальной величины регистрируемого сигнала от величины перенапряжения кремниевых детекторов.

Ключевые слова: SiPM, кремниевые фотоумножители, считывающая электроника, IACT

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Introduction

Currently, the TAIGA Observatory [1] designed to study cosmic sources of gamma-ray emission and cosmic rays is actively developing in the Tunka Valley. This observatory includes an array of Cherenkov imaging gamma-ray telescopes TAIGA-IACT [2], whose detecting chamber is based on vacuum photomultipliers [3]. However, development of microelectronics makes it possible to create detection systems based on silicon photomultipliers, which are superior to vacuum photomultipliers in a number of important parameters. For example, silicon photomultipliers operate at lower supply voltages, are not sensitive to magnetic fields, are more compact and resistant to illumination.

In recent years, the Ioffe Institute has been developing a detector cluster for the camera of TAIGA-IACT based on silicon photomultipliers (SiPM) MicroFJ-60035, sensitive to radiation in both visible (300–600 nm) and ultraviolet (250–300 nm) ranges. The choice of this type of SiPM is due to their high detection efficiency (PDE) both in the visible range (25–50% at an overvoltage of 6 V, depending on the wavelength) and in the ultraviolet range (5–20%, depending on the wavelength). The latter circumstance is important, since the design of the upgraded chamber assumes the possibility of performing rough spectrometry of the Cherenkov radiation of extensive atmospheric showers (EAS) [4], which can increase the efficiency of determining the type of the primary particle (the so-called gamma-hadron separation). In addition, an important feature of these detectors is the presence of a fast output that allows one to obtain a signal length of the order of several nanoseconds, which is important for revealing a low-amplitude signal against a highly noisy background created in the detecting cameras by the night sky radiation.

The development of a new detector cluster is at the final stage; this article describes the final version of the cluster and its testing in a dark chamber.

Description of the cluster

A simplified block diagram of the detector cluster is shown in Fig. 1. The cluster contains 28 pixels based on silicon photomultipliers (SiPM) MicroFJ-60035. The final scheme for removing the signal from the detectors is somewhat different from that described in paper [5]. Each pixel contains four SiPMs. The signals from their fast outputs are fed to the emitters of the BFT93 transistors employed in the scheme with a common base. This switching scheme ensures formation of a short signal. The transistor collectors are connected together, which allows summing up the signals from the detectors before amplifying them and this significantly reduces the number of preamp components, its power consumption and heat dissipation. The pixel preamp has a fixed gain of 100, which is achieved using two gain stages based on AD8099 operational amplifiers with a gain of 10 for each stage. The gain of the entire pixel is changed by adjusting the overvoltage of the silicon photomultipliers.

The signal from each pixel is transmitted via a coaxial cable through high-frequency miniature MMCX connectors and is received by an amplifier stage based on an AD8099 operational amplifier with a total gain of 0.33, which allows the signal to be scaled to the input range of the DRS4 analog memory chip (from 0 V to 1 V).

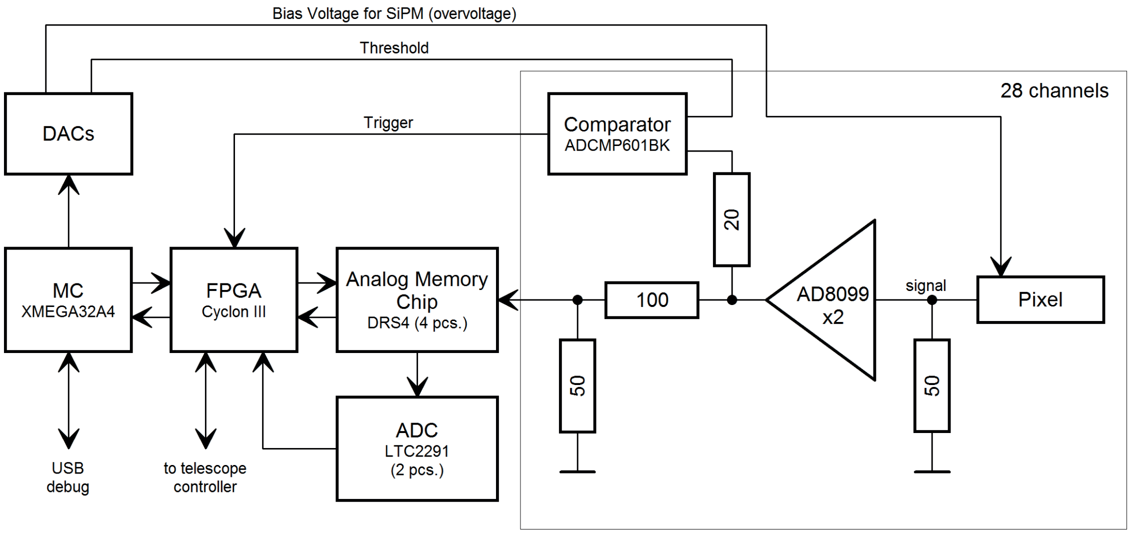

Fig. 1. Block diagram of the detector cluster

Four DRS4 analog memory chips are installed into the cluster. In every DRS4 chip seven channels out of nine are employed. DRS4 is capable of storing a signal with a frequency of up to 5 GHz. Frequency control was tested using a reference frequency and an internal PLL. However, with such a control, some DRS4 chips under the same conditions worked unstable. Therefore, frequency control was implemented by applying a controlled voltage from a digital-to-analog converter (DAC) to the DSPEED input, and this solution was shown to allow a reliable control of the DRS4 frequency and reduce the number of digital signals that can negatively affect the quality of the analog signal from the pixels.

To digitize the signals recorded in the analog memory, two 12-bit two-channel analogtodigital converters (ADC) LTC2291 operating at a frequency of 20 MHz are used. Each ADC digitizes signals from two DRS4 chips.

The control of the DRS4 chip and of accumulation of the digitized signals from the four ADCs is done with a field-programmable gate array (FPGA) Cyclone III, operating at a reference frequency of 100 MHz, while its individual parts operate at a frequency of 400 MHz. The internal memory capacity of the FPGA allows one to record 1024 values with a bit depth of 12 bits for each of the 28 registration channels. However, it is worth noting that each memory cell of the DRS4 chip is characterized by an individual base offset of the zero level different from other memory cells, which can be corrected, and that significantly improves the accuracy of the digitized signal. Tests have shown that without the offset correction, the standard deviation of the channel noise track on average across all the channels is 34 ADC code units, and with the offset correction it reduces to only about 12.5 ADC codes, that is, the noise parameters are improved almost by the factor of 3. However, in order to make such a correction in the FPGA memory, it is necessary to have an array of 1024 numbers for each channel with an individual offset value in order to compensate the values in the real time during signal processing. Unfortunately, the internal memory of the Cyclone III is not enough to store the offset correction values of all the 28 channels, but this can be done at a post-processing step while analyzing the recorded waveforms on a computer.

The data recorded in the FPGA memory are read using an XMEGA microcontroller operating at a frequency of 32 MHz. The microcontroller performs the general command control of the clusters, and also calculates the signal amplitude for each pixel after measurement, and stores the amplitude data in its memory. On a demand from an external computer, the microcontroller transmits the 28 amplitude values. This makes it possible to significantly reduce the amount of data transmitted, since it is not necessary to transmit the channel waveforms. The microcontroller also controls digital-to-analog converters (DACs) over SPI, which set the bias voltage of the detectors, the voltage that determines the frequency of operation of the DRS4, and the threshold voltage of the comparators.

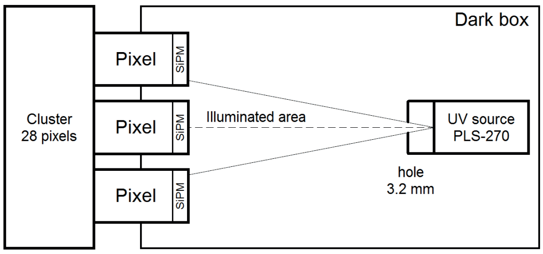

Fig. 2. Scheme of the experiment in the dark chamber

Each of the 28 channels has an ADCMP601BK comparator, which generates a trigger signal when the software-set threshold is exceeded by a signal from a pixel. Each trigger signal of the channel enters the FPGA, which forms a time window of 10 ns for each trigger signal and counts the number of overlaps of the time windows of the channels with each other. If the number of such overlays exceeds a predetermined number, the FPGA generates a stop signal with some delay necessary to write the signal to the memory of the DRS4 chips and starts reading the DRS4 chips. After reading, the FPGA notifies the microcontroller of the completion of the measurement, which either reads the waveforms to determine the amplitudes of the signals, or transmits the waveforms to the computer via an USB connection.

To test the entire cluster in conditions close to working conditions, a dark chamber was developed (Fig. 2).

There is an LED source of UV radiation PLS-270 in the dark chamber, which emits weak pulses of UV radiation at the wavelength of 277 nm, duration of 600 ps and frequency of 5 MHz. A spatial filter with a ⌀3.2 mm hole is installed on the source, which allows one to illuminate certain pixels of the cluster by changing the distance between the silicon detectors and the source. The main part of the cluster is located outside the dark chamber, which contributes to the natural cooling of the electronics. An example of visualization of the data received from the cluster is shown in Fig. 3.

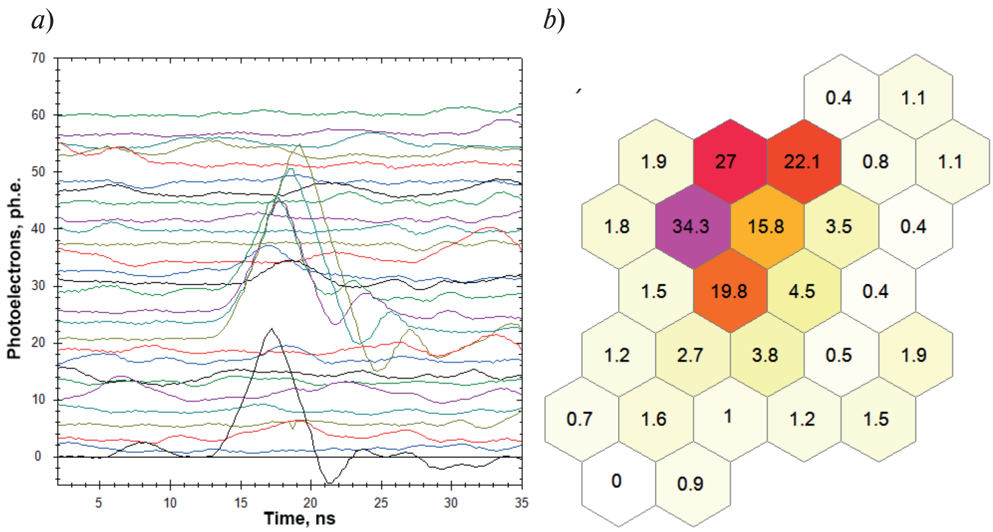

Fig. 3. An example of waveforms (*a*) and an image (*b*) of a UV radiation pulse from a PLS-270 source. The waveforms are artificially shifted relative to each other for clarity. The numbers inside the pixels are the signal amplitudes in photoelectrons (ph.e.)

Calibration of the cluster

The purpose of calibration of the detector cluster is to determine the conversion coefficient of the ADC value (hereinafter code) into the number of photons per pixel, as well as to determine the value of the maximum recorded signal - the maximum range of the cluster. The registration efficiency of silicon photomultipliers, as the ratio of the number of photons registered by the detector to the number of photons that hit the detector, depends on the temperature conditions [6] and on the overvoltage of the detector. Hence, it is advisable to determine the conversion coefficient relative to the number of registered photons (hereinafter referred to as photoelectrons or ph.e.).

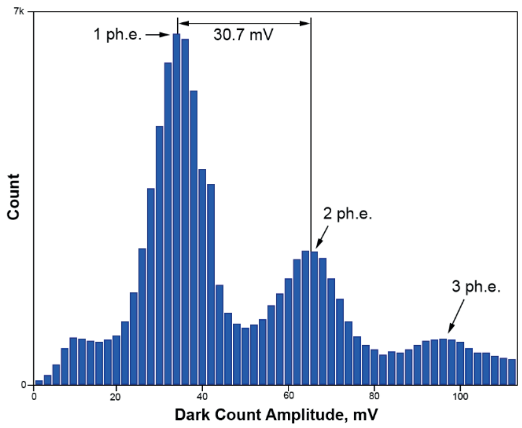

Fig. 4. The amplitude spectrum of the dark count at an overvoltage of 6 V

The detector converts photoelectrons into the signal amplitude in voltage units. This signal is amplified later by the amplifying path and eventually digitized on the ADC, which converts the voltage into a digital code. The described transformation can be reduced to the following formula:

$$K = k_{SiPM} \cdot k_{PA} \cdot k_{Amp} \cdot k_{ADC},$$

where K is the conversion coefficient of the cluster, code/ph.e., k_{SiPM} is the conversion coefficient of silicon photomultipliers in mV/ph.e., k_{PA} is the pixel conversion coefficient (the preamp part of the amplifying path) equal to 100, k_{Amp} is the conversion coefficient of the amplifying path equal to 1/3, k_{ADC} is the conversion coefficient of ADC LTC2291, equal to 4.096 code/mV.

To find the SiPM conversion coefficient at high overvoltage values (above 4.5 V), it is sufficient to measure the difference between the dark count pulses with an amplitude of 1 ph.e. and 2 ph.e., i.e. a single signal that is numerically equal to the conversion coefficient of a silicon photomultiplier. An example of the amplitude spectrum for an overvoltage of 6 V is shown in Fig. 4.

However, when the overvoltage value decreases, the amplitude peaks corresponding to pulses of 1 ph.e. and 2 ph.e. merge, which does not allow one to obtain the value of a single signal directly at low overvoltage values (below 4.5 V). At the same time, it is known that the dependence of the avalanche photodiode gain on overvoltage is linear and can be found in the datasheet of the SiPM from the manufacturer [7]. Therefore, it is possible to extrapolate the trend of the SiPM conversion coefficient to the region of low overvoltage values. Fig. 5 shows the directly measured values of single signals (blue crosses) and a graph of the dependence of the gain of the silicon photomultiplier (red line) on the overvoltage.

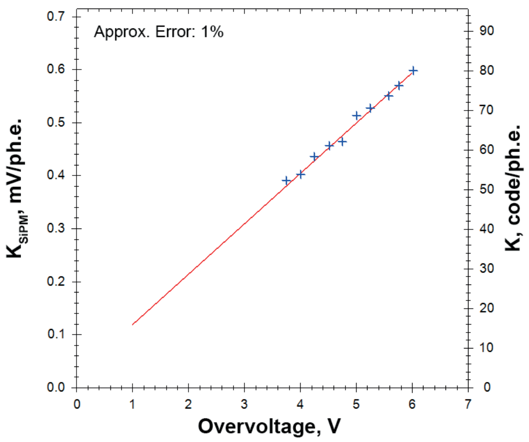

Fig. 5. Dependence of the conversion coefficient of the SiPM and the cluster as a whole on the overvoltage of the detectors

The gain in this graph is renormalized relative to the magnitude of a single signal at an overvoltage of 6 V. The average approximation error of the measured points to the line is 1%. Thus, the cluster conversion factor is 16 code/ph.e. at 1 V of overvoltage and 80 code/ph.e. at 6 V.

Taking into account that the maximum range of the ADC is 4096 codes, and the base signal level of each pixel is shifted by 750 codes, it is possible to determine the maximum range of signals recorded by the cluster in photoelectrons. However, when the overvoltage changes, the registration efficiency (PDE) and the probability of crosstalk also change, therefore, when considering the maximum range of the cluster, it is also important to consider it in photons that have hit the detector. In the silicon photomultiplier datasheet, the manufacturer provides a linear dependence of the PDE on overvoltage, the dependence of the crosstalk on overvoltage is not directly given, but it is reasonable to believe that it is linear based on studies of an analogous MPPC manufactured by Hamamatsu [8].

Fig. 6 shows the dependencies of the maximum range of the cluster in the units of photoelectrons (red line) and in the units of photons (blue line), with account of the PDE and of the crosstalk probability at a given overvoltage. It is worth noting that the microcells of a silicon photomultiplier triggered by a crosstalk can also generate crosstalk events, but here such chains of crosstalk events are not considered.

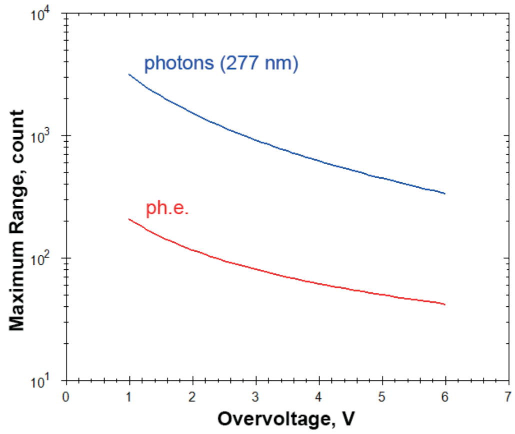

Fig. 6. Dependence of the maximum recorded signal value on the overvoltage of the detectors

At an overvoltage of 6 V, the maximum range of the cluster is 42 ph.e., or 340 photons with a wavelength of 277 nm, and at 1 V is 210 ph.e., or 3200 photons. With a further decrease in the overvoltage below 1 V, a further increase in the range is also expected, however, the approximation of the bias voltage to the breakdown voltage of the silicon photomultiplier may affect the dependencies of the SiPM characteristics and requires a separate dedicated study.

Conclusion

A new experimental detector cluster based on silicon photomultipliers has been developed for the TAIGA-IACT Cherenkov gamma-ray telescope. The signal readout and preprocessing scheme has been worked out. In the calibration process, the dependency of the cluster conversion coefficient on the overvoltage of the silicon detectors was obtained in order to calculate the number of registered photons. The dependency of the magnitude of the maximum recorded signal on the overvoltage of the detectors is obtained as well.

The performed studies complete the stage of development and construction of the detector cluster. In the near future, it is planned to install the cluster into the camera of the currently operating TAIGAIACT unit and carry out observations of the background signal and the signal from bright cosmic gamma-ray sources.

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