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Temperature distribution in InAsSbP/InAsSb/InAs double heterostructure on-chip sensors

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Abstract. The paper presents temperature distribution analysis in activated on-chip chemical sensor based on p-InAsSbP/n-InAsSb/n-InAs 1×3 diode array. Temperature distributions were obtained both experimentally with the use of infrared microscopy, by I-V characteristic analysis and by finite element modelling. The simulated temperature values are in reasonable agreement with experimental data, allowing one to establish a relationship between the temperature of active elements of the sensor. The relationship is important for the improvement of chemical analysis accuracy.

Keywords: Temperature distribution, 1×3 diode array, on-chip chemical sensor, mid-IR photodiodes, mid-IR LEDs, modelling, IR microscopy

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Распределение температуры в микрооптопарах на основе двойной гетероструктуры InAsSbP/InAsSb/InAs

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Аннотация. В работе проведен анализ распределения температуры в активированной микрооптопаре, представляющей собой чип из монолитной двойной гетероструктуры p-InAsSbP/n-InAsSb/n-InAs 1×3. Распределения были получены как экспериментально с помощью инфракрасной микроскопии и анализа ВАХ, так и с помощью моделирования методом конечных элементов. Смоделированные значения температуры удовлетворительно согласуются с экспериментальными данными, что позволяет установить зависимость между температурой активных элементов датчика и важно для повышения точности химического анализа.

Ключевые слова: распределение температуры, микрооптопара, фотодиоды среднего ИК-диапазона, светодиоды среднего ИК-диапазона, моделирование, ИК-микроскопия

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Introduction

Optical chemical sensors are widely used in medicine and industry due to their high reliability and accuracy [1–3]. The expansion of their application areas is facilitated by the use of semiconductor technology, resulting in miniaturized on-chip sensors consisting of an optically coupled diode source and a radiation receiver integrated on a single semiconductor substrate [4–7]. Their operation principle is based on the phenomenon of attenuated total reflection resulting in evanescent wave formation when reflecting light at the interface between the substrate and the analyte. Reflected light intensity recorded by photodiode (PD) is weakening both by analyte absorption and by the angle of total internal reflection increase.

As active part of the sensor (LED) is not solely a source of electroluminescence (EL), but also a source of heat, LED and PD temperature measurements are required to be made especially in miniature or/and monolithic sensors [4, 5]. To improve measurement accuracy in such sensors, it is necessary to know a relationship between the PD and LED temperature. To address this issue, in this work we propose an approach for the above improvement based on a combination of experimental PD temperature values obtained from the analysis of its current-voltage characteristic (*I-V*), infrared (IR) microscope data and results of numerical simulation.

Results and Discussion

We used liquid phase epitaxy grown InAsSbP/InAsSb/InAs heterostructure consisting of n-type InAs (100) substrate with $n = 2 \cdot 10^{16}$ cm^{-3}, ~ 10 μm thick undoped n-$InAs_{1-x}Sb_x$ active (absorbing) layer and p-$InAs_{1-x-y}Sb_xP_y$ (Zn) cladding (contact layer) (see Fig. 1, *b*). The band schematic of this heterostructure and the ability to operate both as PD and LED have been previously described in ref. [8]. The use of the term ‘‘double heterostructure” (DH) is not quite fair in relation to the above heterostructure, but here we use it like in ref. [8].

Diodes were processed onto a 160 μm thick wafer with 26 μm high circular mesas ($Ø_m$ = 190 μm) by standard photolithography and wet chemical etching. Circular Au-based anode ($Ø_a$ = 170 μm) and cathode contacts were formed on the same chip side by sputtering and thermal evaporation in vacuum followed by thick (3 μm) gold plating deposition as shown in Fig. 1, *a*. Chip contained three diodes (the “1×3 linear array”), each diode lateral size was 580×400 μm (see Fig. 1, *a*). Flip-chip bonding/packaging procedure has been implemented using the 2×2 mm submount made from insulating AlN with Cu-Ni-Au metallization at bonding pads, as shown in Fig. 1, *b*. The diodes were connected via a pair of anode (A) – cathode (C) with a number corresponding to the number of the diode (#D1, #D2 and #D3).

To get the temperature distribution on the chip surface (IR map), the IR thermal radiation was mapped using the UTK1 IR microscope developed at the Institute of Semiconductor Physics, Siberian Branch of Russian Academy of Sciences [10]. Temperature distribution from the IR maps was obtained via preliminary calibration that was made in the range of 290–360 K at zero LED current.

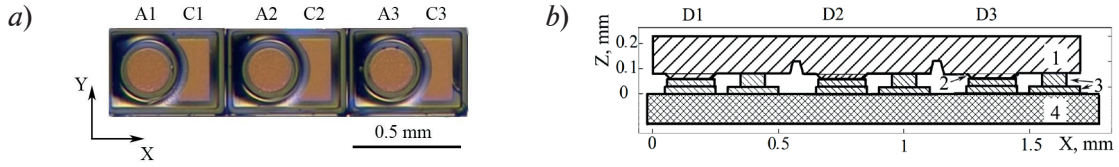

Fig. 1. Top view of the monolithic 1×3 chip (100) surface with three mesas. A1, A2, A3, C1, C2, C3 anodes and cathodes of diodes D1, D2, D3 accordingly (*a*). Schematic diagram of the cross section of the sensor onto submount: 1) InAs substrate, 2) chip active layer and contact layer, 3) solder and submount metallization, 4) AlN based submount (*b*)

Fig. 2 shows IR microscope sensitivity spectrum as well as the EL spectrum of the diodes under study. These spectra do not overlap, and one can expect the absence of the luminescence contribution to the IR maps.

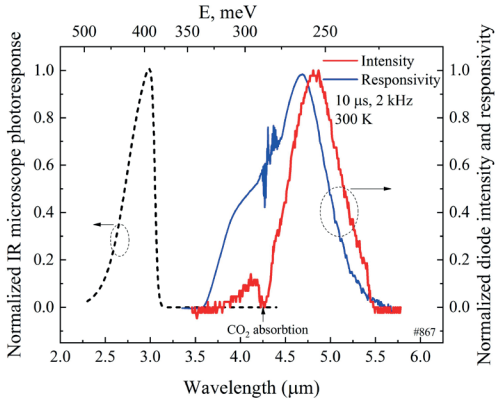

Fig. 2. IR microscope sensor sensitivity (dashed curve) and electroluminescence LED spectrum (solid curve)

The above overlapping absence is confirmed by the measurements of the effective temperature distribution on the chip surface at various ambient temperatures, with forward and reverse D2 bias shown in Fig. 3. The experimental values presented by curves in Fig. 3 are close, which indicates the absence of the EL (at forward bias) and negative luminescence (reverse bias) contribution. The intensity values at 298 K in Fig. 3 are quite "noisy" due to low thermal radiation power; at 323 K this "noise" is not so pronounced because of thermal radiation power enhancement.

The *I-V* characteristics were measured in continuous wave (CW) mode using a SourceMeter Keithley 6430 simultaneously with intensity distribution measurements (intensity maps). During the first part of an experiment the diode D2 was activated, while the *I-V* characteristics were

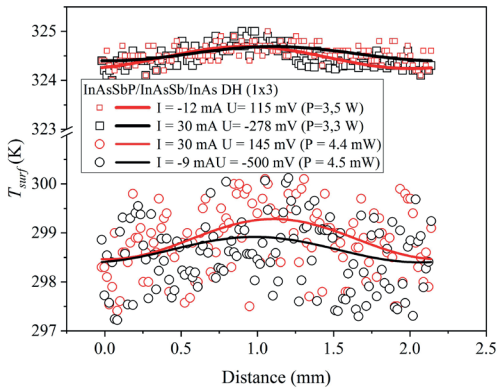

Fig. 3. Temperature distribution along the sensor substrate surface at diode D2 activation (see dots) and curves averaging temperature values obtained from IR maps. The square dot group (□, □) was obtained at a temperature of 323 K, and the round one (○, ○) at 298 K. Red dot/curve data were obtained at forward bias, and black dot/curve data at reverse bias, while the electric power for both modes of operation was the same.

measured in both D1 and D3 diodes, in the second part the diode D1 was activated, and the *I-V* characteristics were measured in the D2 and D3 diodes.

Fig. 4, *a* shows the *I*–*V* characteristics of the diode D1 at various AlN submount temperatures, depicting increase of the current with temperature growth. The temperature dependence of the zero bias resistance R_0 shown in Fig. 4, *b* is described by the standard expression for the diffusion-limited current:

$$R_0 \sim \exp\left(E_a / \left(\beta kT\right)\right), \quad (1)$$

here k is Boltzmann's constant, T is temperature, $\beta \approx 1$, $E_a = 0.26$ eV. The R_0 values obtained from data in Fig. 4, *b* were used to determine the PD temperature.

The thermal conductivities of the sensor layers (Fig. 1, *b*) and their thermal resistances were determined using the "Thermaltester T3Ster" tool (see Fig. 5). Left part of Fig. 5 relates to the diode active and contact layers (item 2 in Fig. 1, *b*), which have a total thermal resistance $R_{th} = 33$ K/W (thermal conductivity K ≈ 24 W/(K*m)). Middle part corresponds to the composite layer consisting of solder, submount metallization and transition sublayer plating-submount (item 3 in Fig. 1, *b*) with a total $R_{th} = 33$ K/W (K ≈ 31 W/(K*m)), and right sector is responsible for the thermal resistance of the AlN submount (item 4 in Fig. 1, *b*) with $R_{th} = 18$ K/W (K ≈ 246 W/(K*m)). The thermal conductivities of the active and contact layers and of the submount are close to the values in [11].

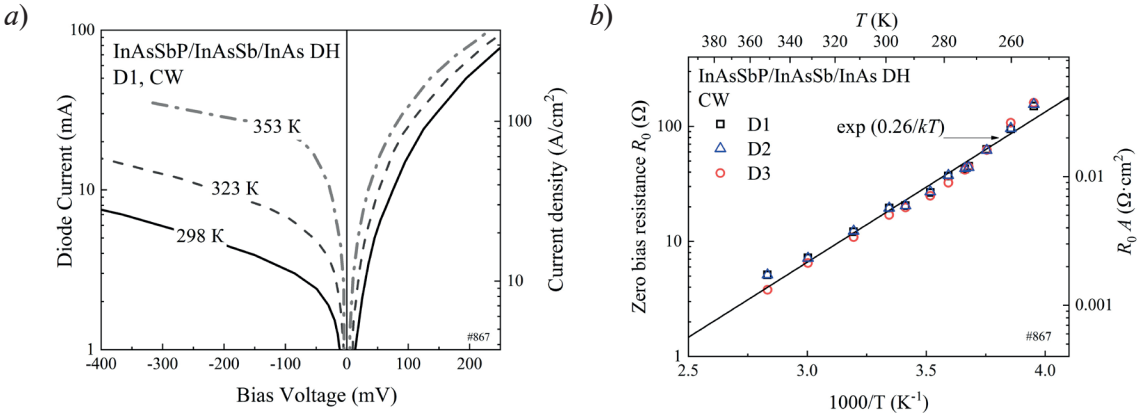

Fig. 4. *I-V* characteristics of D1 diode at various temperatures (*a*). Temperature dependence of zero-bias resistance of the monolithic sensor diodes in the 260–360 K range (*b*)

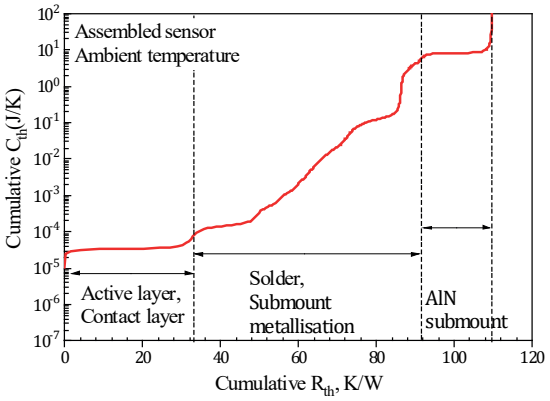

Fig . 5. Cumulative structure functions of assembled sensor including DH layers and submount

In Fig. 6, *a* and Fig. 7, *a* solid lines show the temperature distribution of T_{surf} along the chip surface. The horizontal segments show the average temperature of the active region (item 2 in Fig. 1, *b*) of non-activated diodes (T_{Di}): diode D1 and D3 (Fig. 6, *a*) or diode D2 and D3 (Fig. 7, *a*), obtained from the $R_0(T)$ data. Curves shown in Fig. 6, *a* are asymmetric due to the asymmetry of the on-chip sensor design: the active region of diode D2 is shifted to the right relative to the center of the chip. This "asymmetry" also explains the fact that $T_{D1} > T_{D3}$.

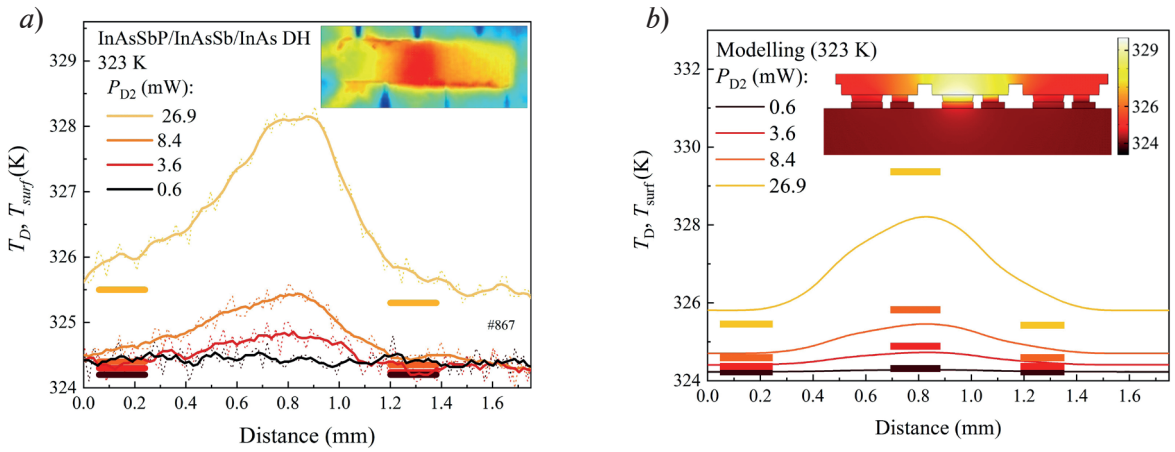

Fig. 6. Temperature distribution on the sensor surface in the center along the X-axis obtained by IR microscope at various electric power applied to diode D2 (solid lines). The temperature of the active region diode D1 and D3 (the segments), from the measurement of R_0. Inset shows an IR map at $P = 26.9$ mW (*a*). The modeled distribution temperature along the chip surface center at various currents in diode D2 (solid lines). The segments are the calculated average temperature of the active regions of diodes. Inset shows the modeled temperature distribution gradients of the sensor cross section (*b*)

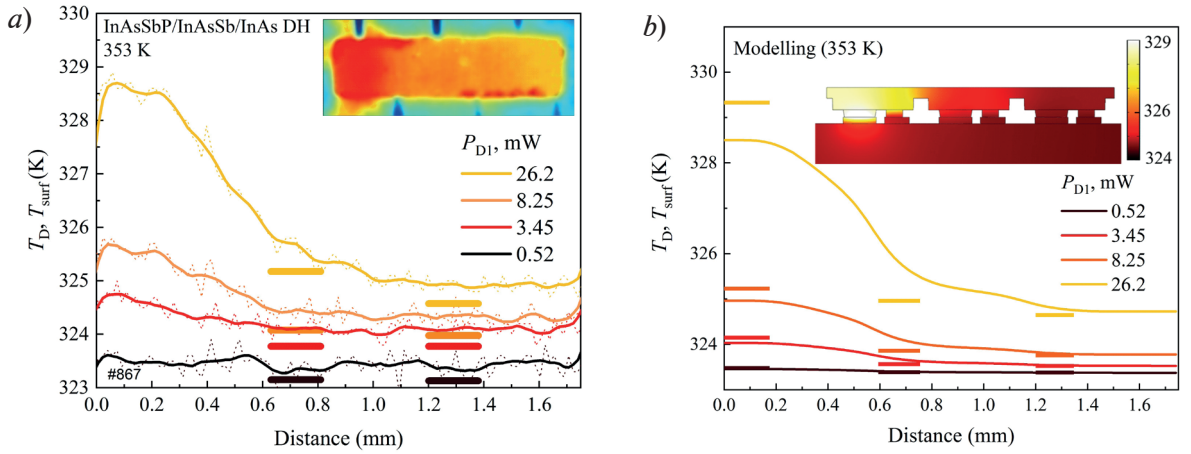

Fig. 7. Temperature distribution on the sensor surface in the center along the X axis obtained by IR microscope at various electric power applied to diode D1 (solid lines). The temperature of the active region diode D2 and D3 (the segments), from the measurement of R_0. Inset shows an IR map at $P = 26.2$ mW (*a*). The modeled distribution temperature along the chip surface center at various currents in diode D1 (solid lines). The segments are the calculated average temperature of active regions of diodes. Inset shows the modeled temperature distribution gradients of the sensor cross section (*b*)

Temperature spatial 3D distribution modeling were performed by the finite element method in the Comsol Multiphysics software by solving the stationary heat equation. The geometry of the 3D model repeated the structure shown in Fig. 1, *b*. The thermal conductivities of the active and contact, metallization, and AlN submount were taken from the above measurements (Fig. 5). It was assumed that the electrical power ($P = I \cdot U$) applied to the LED is totally transferred to heat, since LED internal quantum efficiency is less than 10% and most of EL radiation is reflected back at InAs/air interface [9]. Modelling results are shown in Fig. 6, *b* and Fig. 7, *b*, curves and horizontal segments were calculated for the same chip parts as in Fig. 6, *a* and Fig. 7, *a*. The relative mismatch of simulated and experimental values is less than 5%. The ratio between T_D and T_{surf} and the dependence of T_D и T_{surf} on the LED power are nearly the same. The modeled temperature of the cross section given in the inset in Fig. 6, *b* illustrating the temperature distribution along the Z axis in diodes D1 and D3 shows that the temperature at a surface is higher than in active layers, the same is shown in the inset in Fig. 7, *b* for the diodes D2 and D3.

The calculated dependence of (T_D^{LED}- T_D^{PD}) on power appeared to be close to linear, which agrees with the results in ref. [12] and thus it is possible to elaborate simple empiric relationship between the temperature of the LED and PD in the monolithic sensor chip. This relationship will be very useful for future on-chip sensor [4, 5] data corrections.

Conclusion

In on-chip chemical sensor consisting of p InAsSbP/n-InAsSb/n-InAs DH (mesa diameter 190 μm, λ = 4.7 μm) 1×3 diode array (one LED and two PDs) with overall lateral size 400×1700 μm flip-chip bonded on AlN submount thermal resistances/conductivities of the active and contact layer resistances constitute R_{th} = 33 K/W (thermal conductivity K ≈ 24 W/(K*m)), for layer consisting of solder, submount metallization and transition sublayer plating-submount, R_{th} = 33 K/W (K ≈ 31 W/(K*m)), for AlN submount, R_{th} = 18 K/W (K ≈ 246 W/(K*m)).

Finite element modeled temperature was 328.1 K when the middle (central) diode is activated with electrical power of 26.2 mW and 328.5 K when the edge one is activated (electrical power is 26.9 mW) at submount temperature 323 K. It was shown that PD surface temperature is higher by about 0.5 K than in PD active layer at LED power of 26.2 mW. Dependence of the LED temperature and dependence of difference between LED and PD temperatures on the applied power can be approximated by a linear function. The simulated values were close to those obtained from optical measurements with IR microscope.

We believe that the obtained results will be valid for diode arrays of similar geometry and thus will be useful in evanescent wave chemical on-chip sensor calibration algorithm significantly improving the analysis accuracy.

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