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GaN IC E-mode p-channel and n-channel transistors simulation

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Abstract. This article demonstrates TCAD simulation of normally-off p-channel and n-channel transistors based on a p-GaN gate power platform and estimates interconnections between the key parameters of the heterostructure and device behavior, in other words the type of transistor. GaN platform with p-GaN layer has been developed. It will allow to form n-channel and p-channel, normally-on and normally-off transistors on the same wafer in the same technological cycle and to create GaN complementary pair.

Keywords: GaN, high electron mobility transistor, normally-off transistor, complementary pair, integrated circuit

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Моделирование GaN n-канальных и p-канальных нормально-закрытых транзисторов для монолитных схем

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Аннотация. В данной статье продемонстрировано моделирование нормально закрытых p-канальных и n-канальных транзисторов на основе GaN платформы с p-GaN слоем, а также предложена методика оценки типа прибора по его ключевым параметрам гетероструктуры. Разработана конструкция гетероструктуры для формирования GaN платформы с p-GaN слоем, которая позволит формировать приборы различного типа в едином технологическом цикле на единой подложке, а также создать комплиментарную пару на основе GaN приборов.

Ключевые слова: GaN, нормально-закрытый транзистор, HEMT, комплементарная пара, монолитная интегральная схема

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Introduction

In the past time GaN-based devices have been widely used in electronics due to development of GaN technology. Many of the challenges have been decided, for example, formation of normally-off GaN transistor. But there are still problems with high inductance between the gate electrode and driver circuit and power consumption in power electronic systems and circuits. To overcome this problem monolithic integration of driver circuit and power transistor on the same chip is offered in this article.

There has been a number of articles which demonstrate GaN-based power integrated circuits (IC) [1], but they demonstrate integration of two types – normally-on and normally-off – n-channel transistors. These circuits have disadvantage namely static power dissipation. A complementary circuit technology is needed. The technology advantages are reduction of the circuit complexity, zero power consumption, higher noise immunity and linearity [2]. This article demonstrates simulation of epitaxial structure based on p-GaN gate GaN-on-Si platform that have many advantages, such as large wafer size and low cost.

The GaN ICs allow to form high-frequency reliable power supplies with high efficiency and low cost. Also, the circuits can be widely used in AC/DC and DC/DC converters, increasing their efficiency and power density. Developed product will be used in radar systems, equipment for cellular communication systems, radio relay communication lines, navigation, telecommunications.

Materials and Methods

Based on [3–4] the constructions have been simulated. Simulation has been done with Sentaurus Technology Computer Aided Design (TCAD). The heterostructure pre-analysis was carried out on the solution of statistical problem of the charge carrier distribution in the structure basis. In such systems conduction channel is formed in quantum well on the GaN/AlGaN interface. To calculate carrier channel concentration it is needed to solve quantum-mechanical problem, but quite acceptable accuracy is obtained using the simplest approach based on classical equations in the diffusion-drift approximation. Preliminary estimates can be made based only on a static one-dimensional problem solving the Poisson equation. Thus, we can find normally-off transistor behavior conditions, estimate the transistor threshold voltage Vth at which conduction channel is formed.

The problem current transfer is decided to describe the current-voltage characteristics in details [5]. It is known, that calculation of structures including wide gap semiconductor layers, like GaN, has poor convergence. Calculations taking into account the charge carrier heating and the lattice temperature increase are managed to do only in rather narrow range of voltages at the contacts. At the same time results of calculations considering carrier heating have a little differences from results obtained in diffusion–drift approximation at the stage of linear growth of Id (Vd) up to saturation. In our task we will use diffusion–drift approximation and consider relatively low voltages Vd.

First of all, p-GaN gate n-channel transistor has been simulated. The critical thickness of p-GaN layer is about 70 nm. Choosing p-GaN thickness about 100 nm dependence of type n-channel transistor on AlGaN barrier layer (t_b) and Al mole fraction (x) of this layer has been estimated (Fig. 1) as parameters of AlGaN barrier layer are key parameters determining the type of transistor – normally-on or normally-off. The thickness of AlGaN layer should be as small as possible to provide normally-off behavior.

The heterostructure p-GaN (80 nm)/ $Al_{0.23}GaN$ (15 nm)/ GaN channel / AlGaN buffer/ AlN / Si has been chosen as basic. Mg concentration in p-GaN layer is about $10^{18}sm^{-2}$. These parameters provide normally-off behavior of n-channel p-gate transistor.

To form normally-off p-channel GaN FET n+-GaN is grown on top of p-GaN layer. It's structure with two channels of different carriers. Hole-channel is basic and electron-channel is closed as this transistor works at negative voltages. Space charge region (SCR) of n+-GaN/p-GaN

junction provides normally-off behavior of the device but for certain construction. Thickness of n+-GaN layer and its concentration weakly influence on SCR width. The n+-GaN thickness is 50 nm and impurity concentration in it is about 10^{19}sm^{-2}. Dependence of type p-channel device on p- layer thickness and its activated impurity concentration also has been estimated (Fig. 2). Red region is region in which parameters of p-GaN layer might be chosen to form normally-off p-channel transistor so n-channel transistor is normally-off too. Thus, evaluation methodology of device behavior has been developed and optimal heterostructure for complimentary pair has been chosen.

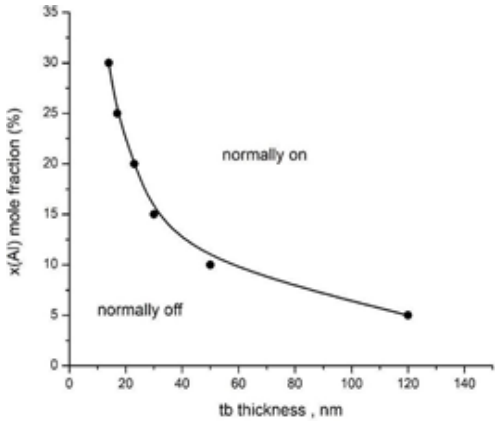

Fig. 1. Dependence of type n-channel transistor on AlGaN barrier layer (t_b) and Al mole fraction (x) of this layer

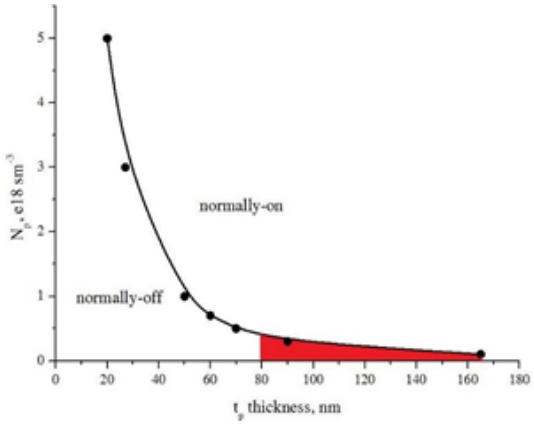

Fig. 2. Dependence of type p-channel device on p-layer thickness and its activated impurity concentration

Results and Discussion

According to the methodology heterostructure design of p-GaN (80 nm)/ $Al_{0.23}$GaN (15 nm)/ GaN channel / AlGaN buffer/ AlN / Si has been chosen. P-GaN gate power platform will include normally-on n-channel transistor, normally-off n-channel p-gate transistor and normally-off p-channel transistor. Simulation of devices shows that the n-channel device with gate length and gate-to-source length about 1 um (Lg = Lgs = 1 um) and gate-to-drain length about 6 um (Lgd = 6um) has threshold voltage Vth is about 1.5 V and maximum drain current in open state is about 400 mA/mm at 4 V on the gate that doesn't contradict our previous result [3]. The p-channel device with gate, gate- to-source and gate-to-drain lengths about 1 um (Lg = Lgs = Lgd = 1 um) has threshold voltage Vth is about -1V and maximum drain current in open state is about -0.9 mA/mm at -3 V on the gate (Fig. 4).

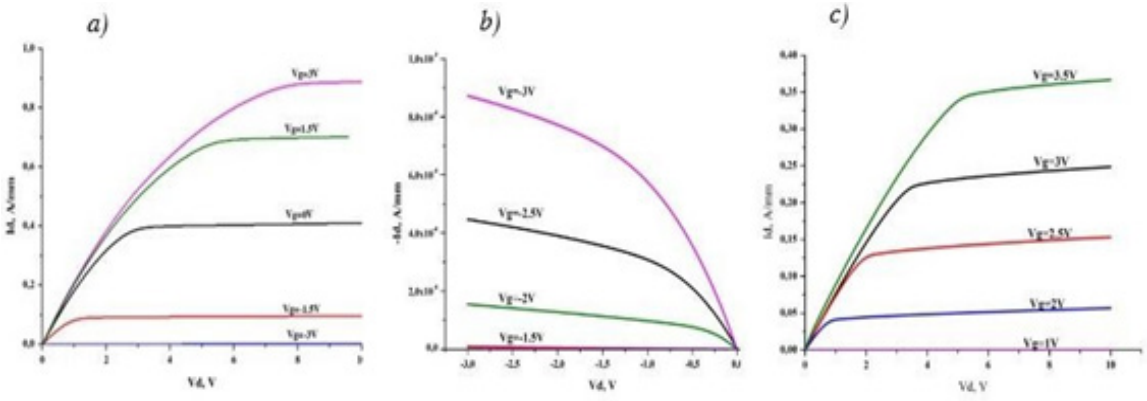

Fig. 4. Current-voltage characteristics of developed devices: *a*) normally-on n-channel HEMT, *b*) normally-off p-channel FET, *c*) normally-off n-channel p-gate HEMT.

Conclusion

Thus simulation of p-gate GaN platform has been demonstrated. It is shown that design of transistor heterostructure can be chosen with proposed methodology. Simulated transistors have an acceptable characteristic and don't contradict our previous result. Such approach allows form different type transistors on the same wafer in a single technological cycle and reduces assembly circuit time.

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