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Effect of pregrowth annealing temperature on the subsequent epitaxial growth of GaAs on Si

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Abstract. In this work, we studied the effect of the pregrowth annealing temperature on the epitaxial growth of GaAs on modified Si area. It is shown that an increase in the annealing temperature leads to a decrease in the selectivity of GaAs epitaxial growth, as well as to a transition from two-dimensional like growth to the growth of nanowires. At an accelerating voltage of 10 kV, 5 passes of the focused ion beam, and an annealing temperature of 600 °C, no epitaxial growth was observed on the modified areas. An increase in the accelerating voltage of the focused ion beam to 20 kV led to the onset of the formation of GaAs nanostructures at low values of the number of passes. An increase in the annealing temperature to 800 °C with the subsequent growth of GaAs leads to the activation of parasitic growth outside the modification regions over the entire range of accelerating voltages and the number of processing passes of the focused ion beam.

Keywords: silicon, gallium arsenide, molecular beam epitaxy, annealing, scanning electron microscopy, focused ion beam

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Влияние температуры предростового отжига на последующий рост арсенида галлия на кремнии

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Аннотация. В данной работе исследовалось влияние температуры предростового отжига на эпитаксиальный рост GaAs на модифицированных участках Si. Показано, что повышение температуры отжига от 600 до 800 °C приводит к снижению селективности эпитаксиального роста GaAs, а также к переходу от двумерного роста к росту нитевидных нанокристаллов.

Ключевые слова: кремний, арсенид галлия, молекулярно-пучковая эпитаксия, отжиг, сканирующая электронная микроскопия, фокусированный ионный пучок

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Introduction

With its high-speed data processing capability, outstanding thermal performance, and low cost, silicon technology is the world leader in modern micro- and nanoelectronics. On the other hand, the indirect-gap nature of silicon does not allow it to be used as a basis for creating information transmission devices based on light sources. For these purposes, III-V semiconductors are used because of their outstanding optical properties. Therefore, in recent years, the task has been to find approaches for the integration of III-V semiconductors on silicon, which would allow combining the advantages of both technologies [1].

The formation of high-quality III-V structures on silicon still remains an unsolved task. One of the important tasks is the problem of mismatch of crystal lattice parameters between silicon and III-V materials, which prevents the monolithic integration of potential photonic integrated circuits based on silicon and III-V light emitting sources [2]. However, not only the difference in the lattice parameters of both materials affects the quality of resulting structures, but also the difference in thermal expansion coefficients [3], as well as the growth of a polar semiconductor on a nonpolar substrate [4].

Recently, many different growth and non-growth techniques have been used for monolithic integration: growth of nanowires (NW) [5], nanoinsertions [6], the use of misoriented substrates [7], aspect ratio trapping [8], etc. [2, 4, 9]. One such method is surface treatment with a focused ion beam (FIB). It is known from the works that this method is used to obtain NWs and makes it possible to create nucleation centers and localize the growth of structures [10, 11]. Also, by changing the parameters of FIB processing and subsequent annealing, it is possible to obtain amorphous and porous areas on a silicon substrate, which will potentially make it possible to reduce the defectiveness of the grown III-V structures [12, 13].

In this work, we study the influence of the annealing temperature of Si(100) modified by FIB on the subsequent GaAs epitaxial growth.

Materials and Methods

Experimental studies of GaAs epitaxial growth were carried out on FIB-modified Si(100) substrates. FIB modification was carried out by treating substrate areas 5×5 μm in size with a Ga^+ beam with an accelerating voltage of 10 and 20 kV and beam passes varying from 5 to 200 (the implantation dose increased accordingly). Then the samples were placed in a growth chamber and subjected to annealing followed by epitaxial growth. The annealing temperature varied from 600 to 800 °C, the annealing time was 60 minutes. Next, a GaAs buffer layer 200 nm thick was deposited at a growth temperature of 600 °C and a growth rate of 0.25 ML/s. Then the samples were removed from the chamber and examined by scanning electron microscopy.

Results and Discussion

At the first stage of experimental studies, samples were obtained annealed at 600 and 800 °C. Fig. 1 shows a significant difference in the morphology of the FIB-modified areas after annealing. Upon annealing at 600 °C, the formation of GaAs structures nanosized arrays is observed on the surface of the modified areas treated at 20kV (Fig. 1, *a*), and upon annealing at 800 °C, holes are formed (Fig. 1, *b*). An explanation of this mechanism of change in the surface structure during annealing is presented in our previous work [12]. However, on surfaces treated with a 10 kV

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beam, a slightly different result is observed. Annealing of such modified surfaces at 600 °C and beam passes number of 200 resulted in the formation of a high-density array with smaller GaAs crystallites (Fig. 1, *c*) than when processed with 20 kV. Increasing the annealing temperature to 800 °C did not lead to the formation of large holes in the modified 10 kV areas (Fig. 1, *d*), as in the case of beam treatment at 20 kV. This behavior is associated with a decrease in the distortion of the Si crystal lattice due to a simultaneous decrease in the ion energy and the implantation dose during FIB treatment at 10 kV.

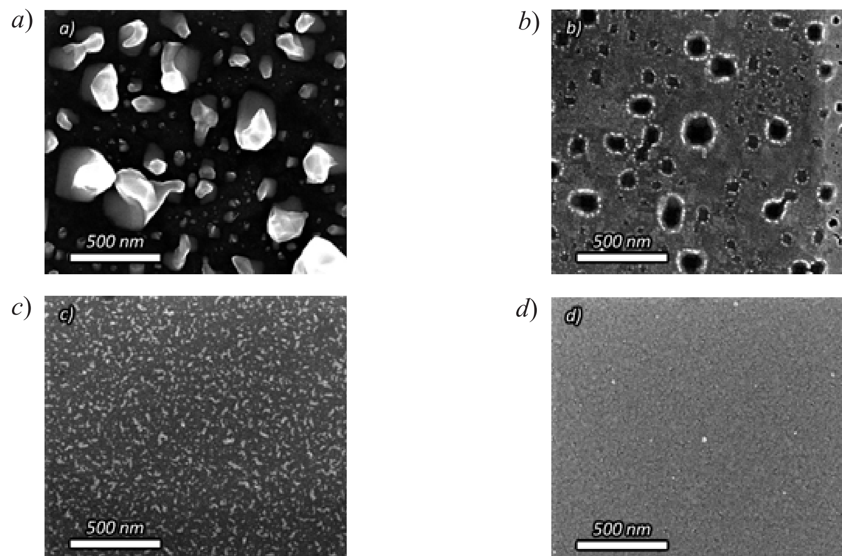

Fig. 1. SEM images of FIB-modified Si areas after annealing in arsenic flux at temperatures of 600 °C (*a*), (*c*) and 800 °C (*b*), (*d*) .The accelerating voltage was 10 kV for (*a*), (*b*), and 20 kV for (*c*), (*d*). The number of beam passes was 200.

At the second stage, the epitaxial growth of GaAs on Si was performed. The results showed the possibility of achieving high selectivity of GaAs growth on FIB-modified samples annealed at 600 °C. A comparative analysis of the structures formed in areas with different FIB exposure modes (Fig. 2) allows us to conclude that the selectivity of the growth process is determined by the number of passes within one value of the accelerating voltage. This can be associated with an increased amount of implanted material. Thus, after deposition of 200 nm GaAs, structures were not formed only in the areas processed at the lowest number of passes and accelerating voltage equal to 10 kV (Fig. 2, *a*). We attribute this behavior to the fact that, at such a number of passes, the formation of nanosized holes on the silicon surface during annealing begins, which act as localization and nucleation centers for epitaxially grown structures.

Note that there is also a difference in the morphology of the obtained structures grown in the areas obtained at 10 and 20 kV. Structures grown in areas with large crystallites (Fig. 1, *a*) end up with a morphology with NWs (Fig. 2, *d*), while such a structure is not observed during growth in areas treated at 10 kV over the entire range of beam passes (Fig. 2, *a*, *b*). This is due to an increase in the total implantation dose with a change in the accelerating voltage from 10 to 20 kV due to an increase in the beam diameter during FIB treatment. This was also affected by the damage of the crystal lattice during processing with higher ion energy, since NWs tend to parasitic growth on defects. Also, by increasing the accelerating voltage to 20 kV during FIB treatment and, in fact, the total dose of implantation, the onset of epitaxial growth is shifted to the region of low beam passes. (Fig. 2, *c*).

Raising the annealing temperature to 800 °C (Fig. 3) followed by the growth of GaAs under similar conditions leads to the activation of parasitic growth outside the modification areas, which reduces the selectivity of the growth process. This change is associated with the formation of pores in the native oxide at a high annealing temperature. It should be noted that the growth of GaAs in the modified areas is accompanied by the formation of nanowires oriented in directions perpendicular to each other. Increasing the accelerating voltage to 20 kV led to a change in the GaAs morphology in the modified area and the formation of a distinct structure already

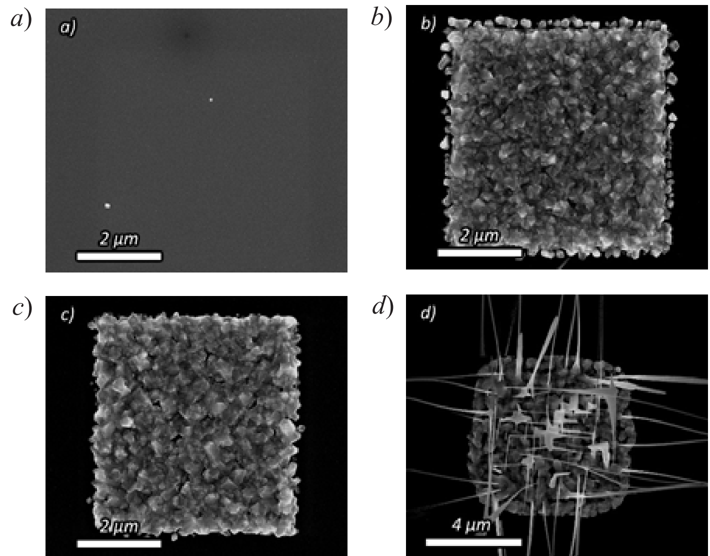

Fig. 2. SEM images of FIB-modified Si areas after annealing at $T = 600$ °C followed by deposition of 200 nm GaAs at $T = 600$ °C. The number of beam passes was 5 for (*a*), (*c*) and 200 for (*b*), (*d*). The accelerating voltage was 10 kV for (*a*), (*b*), and 20 kV for (*c*), (*d*)

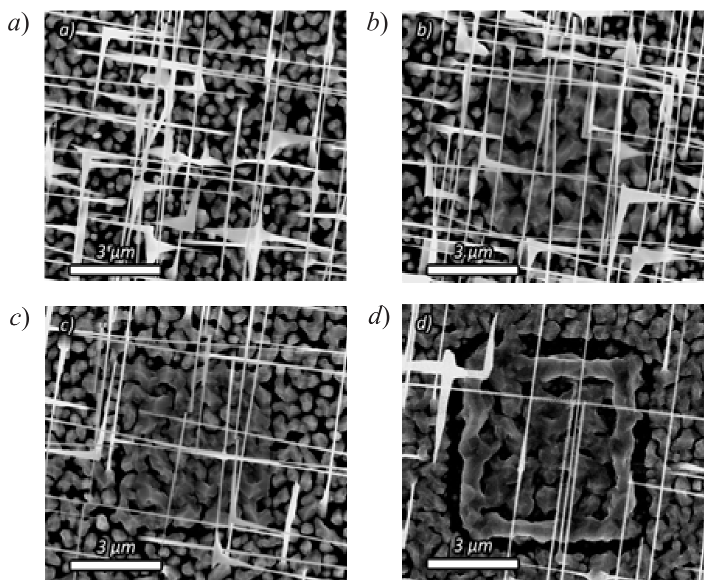

Fig. 3. SEM images of FIB-modified Si areas after annealing at $T = 800$ °C followed by deposition of 200 nm GaAs at $T = 600$ °C. The number of beam passes was 5 for (*a*), (*c*) and 200 for (*b*), (*d*). The accelerating voltage was 10 kV for (*a*), (*b*), and 20 kV for (*c*), (*d*)

at low number of beam passes (Fig. 3, *c*). However, the presence of parasitic growth outside the modification areas is an undesirable result, so annealing at 600 °C is more optimal for the localization of the GaAs nanostructure.

Conclusion

It can be seen from the above results that changing the annealing temperature, accelerating voltage, and/or the number of passes makes it possible to obtain various kinds of morphology on the silicon surface: from the formation of a surface with GaAs crystallites to strongly disturbed with the formation of holes. The influence of these parameters on the subsequent epitaxial growth is great, since they allow one to change not only the morphology of the resulting structures, but also the type of growth. However, further research in this direction is required to identify the optimal set of GaAs growth parameters on FIB-modified Si (growth rate, V/III flux ratios, deposition thickness, etc.).

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