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# Improvement of the characteristics of the frequency synthesizer in the quantum frequency standard on caesium-133 atoms

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**Abstract.** A new circuit of a frequency synthesizer is presented, which is an important functional node in the quantum frequency standard on cesium atoms. The advantages and disadvantages of the new signal synthesis method are considered in detail. By increasing the bit depth of the accumulating adder, it was possible to reduce the step of tuning the output frequency by several orders of magnitude. This method meets all the requirements for the parameters of frequency synthesizers.

**Keywords:** quantum frequency standard, frequency synthesizer, direct digital synthesis, accumulating adder, frequency tuning, cesium atomic clocks

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# Улучшение метрологических характеристик синтезатора частоты для квантового стандарта частоты на атомах цезия-133

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**Аннотация.** Представлена новая схема синтезатора частот, который является важным функциональным узлом в квантовом стандарте частоты на атомах цезия. Подробно рассмотрены достоинства и недостатки нового метода синтеза сигнала. С помощью увеличения разрядности накапливающего сумматора удалось добиться уменьшения шага перестройки выходной частоты на несколько порядков. Сделан вывод о том, что данный метод удовлетворяет всем требованиям, предъявляемым к параметрам синтезаторов частоты.

**Ключевые слова:** квантовый стандарт частоты, синтезатор частоты, прямой цифровой синтез, накапливающий сумматор, перестройка частоты, цезиевые атомные часы

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## Introduction

The frequency can be determined with the greatest precision among all physical quantities [1–8]. The development of frequency measurement methods has increased the accuracy of measuring quantities that can be determined through it [1, 3, 4, 7–14]. The international system of units, using physical laws and fundamental constants, defines other units of measure in terms of seconds. Frequency standards are often used as reference standards [1, 3, 4, 15–22]. The frequency standard is a source of electromagnetic pulses that generates the desired frequency signal with a given accuracy and provides the consumer with frequency references from a wide range. The 1 second time standard is defined in world science as the time interval during which 9,192,631,770 periods of electromagnetic radiation occur during the transition between two hyperfine levels of the fundamental state of the $^{133}$Cs atom. That is why the $^{133}$Cs frequency standard was used as the primary reference on the basis of which the international time scale is based [1, 15, 22–26].

The first frequency standard for $^{133}$Cs was developed in the mid-20th century. It is this standard which, unlike others, has a precise unit of time and a uniform time scale. Since then, the quantum frequency standard on cesium atoms has been modified due to the development of electronics, materials, and more. The diagram of quantum frequency standard on $^{133}$Cs is given in Fig. 1.

Quantum frequency standards are divided into two types. Active quantum standards emit

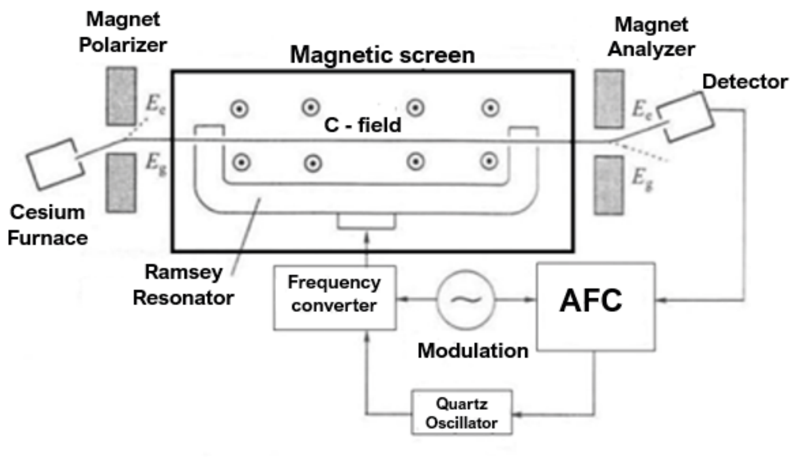


Fig. 1. Diagram of cesium atomic clock

electromagnetic waves, the frequency of which is determined by the spectral line of matter. Such devices are also called quantum generators. In passive quantum standards, the measured oscillation frequency of the external generator is compared to the spectral line frequency. Cesium atomic clocks are passive quantum frequency standards.

One of the important functional nodes of the quantum frequency standard is the frequency synthesizer [26–33]. The synthesizer is a source of stable fluctuations in devices that require tuning to different frequencies in a wide range and high stability of the selected frequency. It should be noted that the accuracy of the output signal generated by the synthesizer affects the accuracy of the transition resonance frequency and other characteristics of the quantum standard output signal. Therefore, in the context of increasing requirements to the frequency standard, this issue requires increased attention. One of the solutions is presented in our work.

## Materials and Methods

The most common methods to date are the following methods of frequency synthesis:

**Direct analog synthesis.** This method is called so because it does not have a stage of error correction. Because of this, the accuracy of synthesizer output signal synthesis depends on the quality of input clock. Several support generators are used to quickly change the frequency of the device. The need to synthesize a signal from a wide range of frequencies forces designers to use a large number of support generators. Direct synthesis devices are cumbersome and expensive.

**Indirect synthesis.** This method is based on phase automatic frequency adjustment. The output frequency is formed by an additional generator, which is covered by a loop of phase automatic frequency adjustment. The presence of a phase detector in the synthesizer design causes phase noises. In order to reduce the frequency rearrangement step, it is necessary to work at a low frequency of comparison, which forces to reduce the frequency of the loop filter cutting. It also negatively affects the phase noise of the device. The design of such a frequency synthesizer does not allow for a high rate of frequency adjustment.

**Direct digital synthesis.** This is a relatively new method of frequency synthesis, which appeared in the early 1970s. All described synthesis methods have been available to developers for quite a long time, but only recently has the method of direct digital synthesis been given close attention. This method is special because the generated signal is synthesized with the inherent precision of digital systems.

**Hybrid synthesis.** A synthesis method in which a combination of several previously described methods takes place.

The new design of the digital frequency synthesizer uses the above method of direct digital synthesis. This is due to some advantages compared to other frequency synthesis methods. Digital systems synthesize a signal with precise specified characteristics. The parameters of the output signal, such as frequency, amplitude and phase, are precisely known and continuously controlled by the system. High frequency and phase resolution, fast switching to another frequency and high rate of adjustment in the absence of emissions or other distortions that may occur due to timing, a wide range of generated frequencies are also advantages of this method.

The synthesizer circuit based on this method includes only one unstable element, the digital-analog converter. This instability is common to all analog circuits.

Modern synthesizers use an updated version of direct digital synthesis. For this reason, the ROM address counter has been replaced by an accumulating adder. The accumulating adder is a case, at each stroke of which the device reboots. Also, for each stroke of the device, there is a summation of the value obtained earlier, and the constant - summing with accumulation. The resulting synthesizer diagram is shown in Fig. 2.

The value contained within the register is constantly increasing over time, the value of the

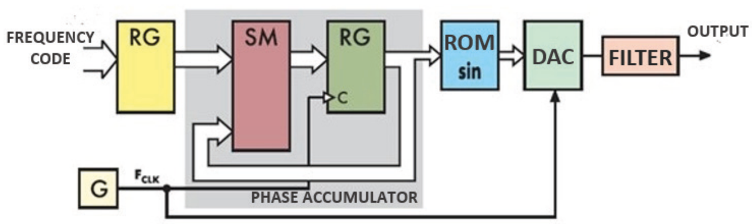


Fig. 2. Digital synthesizer circuit

additive depends on the constant term. At the output of the accumulating adder a code is obtained, which corresponds to the phase of the signal at the current time. The addressable, which is used in the operation of the device, corresponds to the growth of the signal phase in one cycle of operation. The amount of frequency of the synthesized signal is directly proportional to the rate of change of the phase of the signal in time. Thus, the phase increase value corresponds to the binary frequency code at the register output.

So the accumulating adder, also called the phase battery, synthesizes a sequence of binary codes from the linearly changing phase of the signal. The phase battery overflow frequency corresponds to the output signal frequency. The output frequency is determined by the formula:

$$F_{out} = \frac{M \cdot F_{clk}}{2^N},$$

where $F_{out}$ is the output frequency, $F_{clk}$ is the clock speed, M is the binary frequency code, $N$ is the discharge of the accumulating adder.

The frequency represented as a binary code determines the speed at which the signal phase will change. The increasing phase is converted into output signal values, from which the DAC generates a signal of sinusoidal form, consisting of 'steps'. The lower frequency filter smoothes the 'steps', and thus the sinusoidal output signal is formed (Fig. 3).

The signal at the output of the device is created from separate counts. Not always in the sine

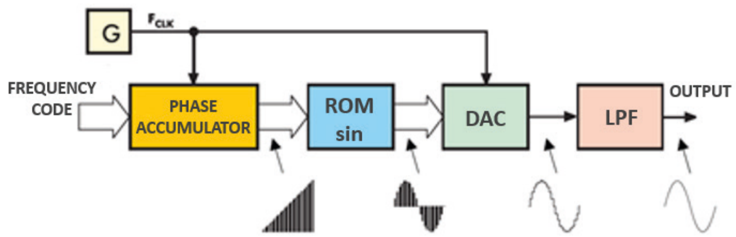


Fig. 3. Principle of the synthesizer

period is placed an integer number of counts. More often than not, the periods are different, differing from previous and subsequent periods. In some cases, it is possible that the location of the readings may be repeated with a certain period, but this period of repetition is very different throughout the signal. This period is determined by a number of factors, such as frequency code, adder discharge and phase code bit. Thus, a sinusoidal signal can be formed from a sequence of readings.

Despite the fact that noise is reduced when the frequency is divided, the main cause of the phase noise in the scheme is the presence of a source of clock signal. In theory, the phase noise of the clock signal is greater than that of the output signal. In fact, noise reduction is limited to the noise threshold of the circuits used, and the phase output reduction is limited to the amount of clock noise. Residual phase noise is the amount of noise below which the output noise cannot be lowered.

**Results and Discussion**

In the course of the study, modeling was carried out in a specialized development tool Quartus II, which is focused on the work with FPGA firm Altera. A program code was written to implement direct digital frequency synthesis in VHDL. The data was loaded from the microcontroller using the peripheral interface SPI (Serial Peripheral Interface). Fig. 4 presents the results of modeling.

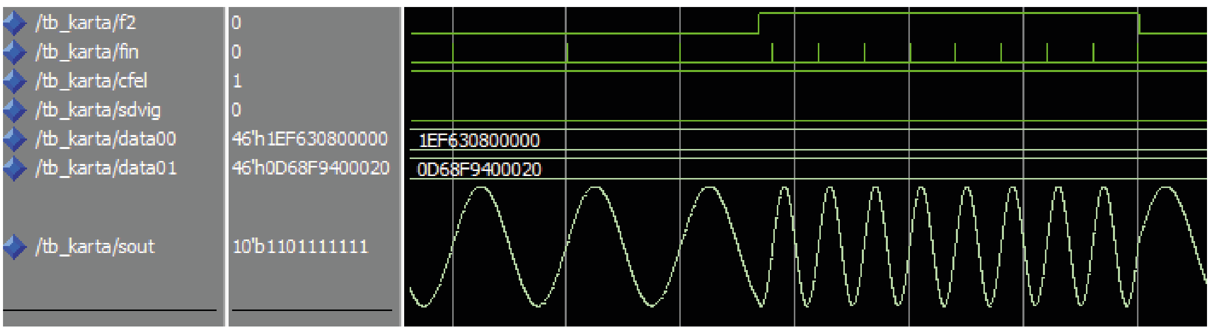


Fig. 4. Simulation result

An earlier version of the synthesizer used a 32-bit phase battery. Increasing the number of discharges of the device to 40 allowed to lower the value of the step of frequency adjustment. The scheme created when operating at 15 MHz has an output frequency change step:

$$\Delta F_{out} = \frac{F_{clk}}{2^N} = \frac{15 \cdot 10^6}{2^{40}} = 1.36 \cdot 10^{-5} \text{ Hz}.$$

When operating at 25 MHz, the rearrangement step will be:

$$\Delta F_{out} = \frac{F_{clk}}{2^N} = \frac{25 \cdot 10^6}{2^{40}} = 2.27 \cdot 10^{-5} \text{ Hz},$$

where $\Delta F_{out}$ is the step of restructuring the output frequency, $F_{clk}$ is the clock speed, $N$ is the discharge of the accumulating adder.

The resulting value of the synthesizer $\Delta F_{out}$ frequency restructuring step is an order of magnitude lower than the value $\Delta F_{out}$ used in previous frequency synthesizer designs.

## Conclusion

The results obtained by tuning the frequency of the synthesizer output signal made it possible to improve several times the accuracy of the formation of the frequency of the microwave excitation signal corresponding to the resonant transition in the atomic structure.

The parameters of the developed frequency synthesizer based on the DDS method (direct digital synthesis) meet most of the new technical requirements for signals in the quantum frequency standard. In addition, most of the parameters of the developed frequency synthesizer are controlled by the program.

The newly developed design of the frequency synthesizer has reduced energy requirements, which is essential for subsequent use.

This frequency synthesizer design can be successfully used in other types of quantum frequency standards (e.g., rubidium-87 atoms, etc.).

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