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Algorithm and installation for measuring the current lacing voltage in high-power RF and microwave bipolar and heterojunction bipolar transistors

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Abstract. Methods of measuring the current lacing voltage in high-power bipolar (BT) and heterojunction bipolar (HBT) RF and microwave transistors are considered. A method and installation for determining the current lacing voltage in a transistor without introducing the device into the hot spot mode by the steepness of the dependence of the variable component of the voltage at the emitter junction on the collector voltage at a given emitter current and the supply of the sum of linearly increasing and small alternating voltage to the collector is described. A critical drawback of the known methods for determining the voltage of the U_{KL} localization in BT and HBT is that the devices enter the hot spot mode thus the purpose of the work was to develop and experimentally test an algorithm and installation for measuring the voltage of the U_{KL} localization without introducing the device into the hot spot mode.

Keywords: microwave bipolar transistor, current lacing voltage, non-destructive method, measurement, installation

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Материалы конференции
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Алгоритм и установка для измерения напряжения локализации тока в мощных ВЧ и СВЧ биполярных и гетеропереходных биполярных транзисторах

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Аннотация. Рассмотрен метод измерения напряжения локализации тока $U_{КЛ}$в мощных биполярных (БТ) и гетеропереходных биполярных (ГБТ) ВЧ и СВЧ транзисторах. Описан метод и установка для определения напряжения локализации тока $U_{КЛ}$ в транзисторе без введения прибора в режим горячего пятна по крутизне зависимости переменной

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составляющей напряжения на эмиттерном переходе от коллекторного напряжения при заданном эмиттерном токе и при подаче на коллектор суммы линейно нарастающего и малого переменного напряжения. Существенным недостатком известных способов определения напряжения локализации $U_{КЛ}$ в БТ и ГБТ является выход приборов в режим горячего пятна, поэтому целью работы являлась разработка и экспериментальная проверка алгоритма и установки для измерения напряжения локализации тока $U_{КЛ}$ без введения исследуемого прибора в режим горячего пятна.

Ключевые слова: СВЧ биполярный транзистор, напряжение шнурования тока, неразрушающий метод, измерение, установка

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Introduction

It is known that current distribution in high-power bipolar (BT), including heterojunction bipolar (HBT), loses stability at certain values of collector voltage of the U_{KL} localization under which the so-called "current cord" and "hot spot" (HS) are formed in the structure of the device [1–4]. The line of mode parameters in current-voltage coordinates corresponding to current lacing defines one of the boundaries of the safe operation area (SOA) of BT and HBT, going beyond which, even for a short time, leads either to irreversible destruction of the instrument structure and catastrophic failure of the device, or to degradation of the device [5]. Even in the absence of irreversible damage, strong overheating of the local region of the structure is accompanied by large thermal deformations, an increase in the number of dislocations and microcracks in the semiconductor, and accelerated MBT degradation.

A critical drawback of the known methods [6–8] for determining the voltage of the U_{KL} localization in BT and HBT is that the devices enter the HS mode thus the purpose of the work was to develop and experimentally test an algorithm and installation for measuring the voltage of the U_{KL} localization without introducing the device into the HS mode.

Materials and Methods

According to the model presented in [9], for the case of defects of an electrophysical nature in the BT structure, the dependence of the variable voltage component $\tilde{U}_{EB}$ on emitter junction from the collector voltage is described by the formula:

$$\tilde{U}_{EB}(U_K) = \tilde{U}_{EB}(0)\left[1 + \frac{b}{\left(1 - U_K / U_{KL}\right)^2}\right], \quad (1)$$

where $\tilde{U}_{EB}(0)$ is the amplitude of the alternating voltage at the emitter junction at a collector voltage U_{K0} close to zero; b – is a dimensionless parameter depending on the magnitude of the defect in the BT structure, and, as a rule, $b << 1$.

Based on this model, in [9] a non-destructive method and in [10] the installation are proposed for determining the U_{KL} at a given emitter current by three counts of the alternating voltage at the emitter at three collector voltages U_{K0}, U_{K1}, U_{K2} of a transistor included in a circuit with a common base, when the sum of a linearly increasing voltage and a small sinusoidal voltage is applied to the collector:

$$U_{\hat{E}L} = \frac{U_{K2} - mU_{K1}}{1 - m}, \quad (2)$$

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where $m=\sqrt{\frac{a1-1}{a2-1}}$, $a1=\tilde{U}_{EB}\left(U_{K1}\right)/\tilde{U}_{EB}\left(U_{K0}\right)$, $a2=\tilde{U}_{EB}\left(U_{K2}\right)/\tilde{U}_{EB}\left(U_{K0}\right)$.

The accuracy of this method strongly depends on the choice of collector voltage values, while there is a possibility of the device entering the HS mode. In order to exclude the devices from entering the HS mode and to increase the accuracy of determining the U_{KL} when setting the transistor mode, the new method proposes to measure the amplitude of the alternating emitter voltage at a low collector voltage; then measure the values of the collector voltage, at which the amplitude becomes equal to (1+k1) and (1+k2), and the voltage U_{KL} is calculated by the formula:

$$U_{KL}=\frac{\sqrt{k2/k1}U_{K2}-U_{K1}}{\sqrt{k2/k1}-1}, \tag{3}$$

where k1 and k2 are the given coefficients of response.

Figure 1 shows a characteristic type of BT dependence with current localization with specified levels, and Figure 2 shows a block diagram of the device implementing the method [11].

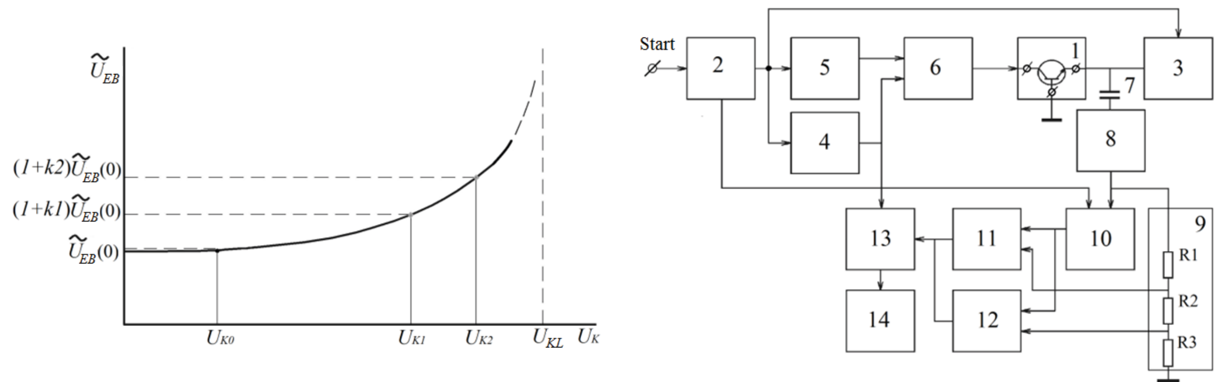

Fig. 1. Type of BT dependence with current localization and preset levels

Fig. 2. Block diagram of the device implementing the method

The device implementing the method contains a block 1 for connecting a transistor; a control device 2; a current source 3; a linearly increasing voltage generator 4; a low frequency generator 5; a power amplifier adder 6; a separating capacitor 7; an envelope extraction device 8; a resistive divider 9; a sampling and storage device 10; comparators 11 and 12; logger 13 and computer 14.

The device works according to the following algorithm. The tested transistor 1 is switched on according to the circuit with a common base. The device works according to the following algorithm. The tested transistor 1 is switched on according to the circuit with a common base. During the action of the control pulse $T_{изм}$ with a duration generated by the control unit 2 at the signal "start", the emitter current I_E is set by the current generator 3, and the sum of the linearly increasing and sinusoidal voltages is applied to the collector from the output of the power amplifier 6:

$$U_K(t) = U_{KM}t\,/\,T_{изм} + U_m \sin \Omega t, \tag{4}$$

generated by the generator 4 linearly increasing voltage and the generator 5 low frequency. The variable voltage component $\tilde{U}_{EB}(t)$ from the emitter of the transistor through the coupling capacitor 7 is fed to the input of the envelope selection device 8, from the output of which the envelope voltage of the variable voltage component at the emitter is fed to the input of the resistive divider 9 and the sampling and storage device 10. According to the second signal of the control device 2 at the time t_0, the sampling and storage device 10 remembers and stores the value of the amplitude of the variable component $\tilde{U}_{EB}(0)$ of the voltage at the emitter junction of the transistor when the collector voltage is close to zero. The voltage from the output of the sampling and storage device 10 is supplied to the first inputs of the comparison devices 11 and 12, the second inputs of which receive signals from the first and second outputs of the resistive divider 9. The resistance values of resistors R_1, R_2 и R_3 are chosen so that the voltage division

factor at the first output of divider 9 is equal to (1+k1), and at the output of the second one it is (1+k2), where k1 and k2 are the given coefficients of exceeding the initial amplitude $\tilde{U}_{EB}(0)$. At times t_1 and t_2, when the voltages at the outputs of the resistive divider will be equal $\tilde{U}_{EB}(0)$ comparison devices 11 and 12 generate short pulses, according to the signals of which the recorder 13 measures the voltages U_{K1} and U_{K2} at the output of the generator 4 and transfers them to the calculator 14, which calculates the desired localization voltage according to formula (3).

Results and Discussion

An experimental sample of the device is implemented on the basis of an Arduino debugging board. The algorithm and the experimental device were tested on transistors of the KT903B type, some of the results are presented in the table 1. The measurements were carried out at an emitter current of 0.8 A, a collector voltage of 50 V, and a measurement time of 2.5 s.

Table 1

The results of determining U_{KL} for transistors of the KT903B type at two values of the coefficient k

No. trans.	U_{K2} at $k2$ = 0.8, V	U_{K1} at $k1$ = 0.5, V	U_{KL}, V
265	43	36	50.8
377	37	36	38.1
971	42	39	45.1
281	37	33	41.4

The use of the algorithm described above and the data processing unit made it possible to measure the dependence of the current lacing voltage on the emitter current for microwave transistors of the KT920B and KT925B types, see Fig. 3.

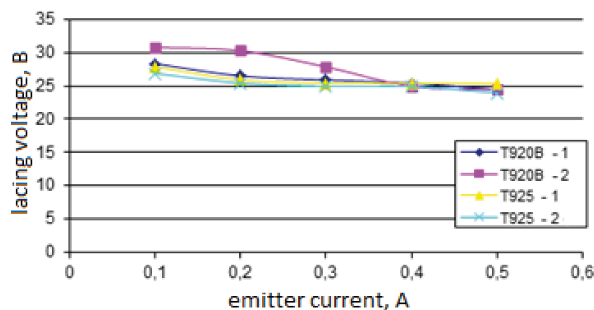

Fig. 3. Dependence U_{KL} transistors type KT920B and KT925B from emitter current

It can be seen from the Fig.3 that at lower emitter currents, the value of the localization voltage differs significantly from sample to sample. At high currents, the localization voltages practically coincide. To increase the reliability of rejection, it is necessary to set small emitter currents, at which the spread of U_{KL} values is greater. These results are consistent with known models of thermal instability in BT and HBT.

Defects that reduce the current lacing voltage also manifest themselves in an increase in the thermal resistance of the HBT. To verify this conclusion, the correlation between the lacing voltage U_{KL} and the thermal resistance R_{TRCB} of the collector-base junction was evaluated on a sample of transistors of the KT840B type; U_{KL} was measured on the described installation at a current of 1.5 A, and R_{TRCB} was measured with a thermal resistance meter at a current of 1.1 A. The correlation coefficient was – 0.45, which confirms, taking into account the influence of other factors, the presence of a rather strong relationship between U_{KL} and R_{TRCB}. By selecting measurement modes, the relationship between the indicated parameters can probably be increased.

Conclusion

Thus, using the described algorithm and installation, it was possible to measure the current lacing voltage localization voltage on several samples of transistors. In addition, it was found that there is some correlation between the voltage of the U_{KL} localization and the thermal resistance of the collector-base junction R_{TRCB}.

The values of collector voltage of the U_{KL} localization in the transistor structure can serve as a measure of defectiveness; therefore, the developed algorithm and installation will be widely used in the field of non-destructive input and output quality control of products at enterprises engaged in the manufacture of electronic equipment.

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